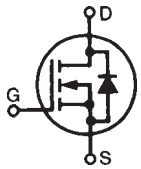
IXYS

Polar™ Power MOSFET IXFR140N30P
HiPerFET™

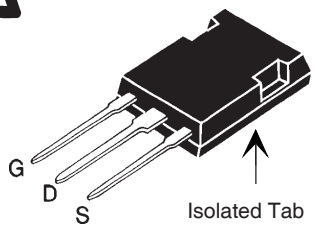
V_{DSS} = 300V
I_{D25} = 70A
$R_{DS(on)}$ ≤ 26mΩ
t_{rr} ≤ 200ns

(Electrically Isolated Back Surface)

N-Channel Enhancement Mode
Avalanche Rated



ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		300	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ		300	V
V_{GSS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C		70	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}		300	A
I_A	T_C = 25°C		70	A
E_{AS}	T_C = 25°C		5	J
dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$		20	V/ns
P_D	T_C = 25°C		300	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6mm (0.062 in.) from case for 10s		300	°C
T_{SOLD}	Plastic body for 10s		260	°C
V_{ISOL}	50/60 Hz, RMS	t = 1min	2500	V~
	$I_{ISOL} \le$ 1mA	t = 1s	3000	V~
M_d	Mounting force		20..120 / 4.5..27	N/lb.
Weight			5	g

Features

- UL recognized package
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA		300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA		3.0		5.0	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V				±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$				25	μA
	V_{GS} = 0V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 70A, Note 1			20	26	mΩ

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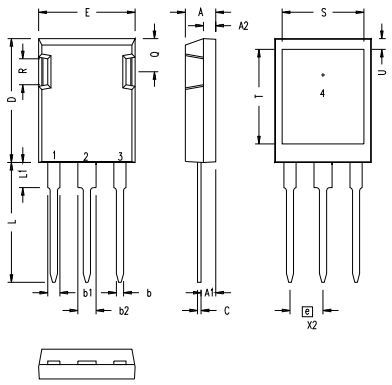
Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	V_{DS} = 20V, I_D = 70A, Note 1	50	90	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		14.8	nF
C_{oss}			1830	pF
C_{rss}			55	pF
$t_{d(on)}$	**Resistive Switching Times**		30	ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 70A		30	ns
$t_{d(off)}$	R_G = 1Ω (External)		100	ns
t_f			20	ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 70A		185	nC
Q_{gs}			72	nC
Q_{gd}			60	nC
R_{thJC}				0.42 °C/W
R_{thCS}			0.15	°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.
I_S	V_{GS} = 0V			140 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			560 A
V_{SD}	I_F = 70A, V_{GS} = 0V, Note 1			1.3 V
t_{rr}	I_F = 25A, -di/dt = 100A/μs			200 ns
Q_{RM}	V_R = 100V, V_{GS} = 0V		0.6	μC
I_{RM}			6.0	A

Note 1: Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

ISOPLUS247 (IXFR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25ºC

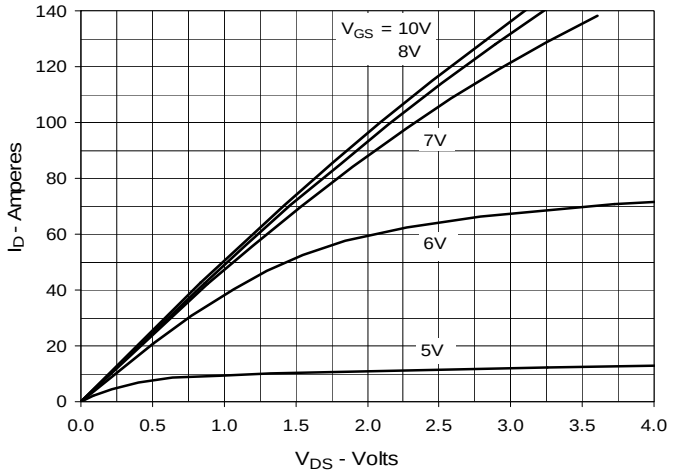


Fig. 2. Extended Output Characteristics @ 25ºC

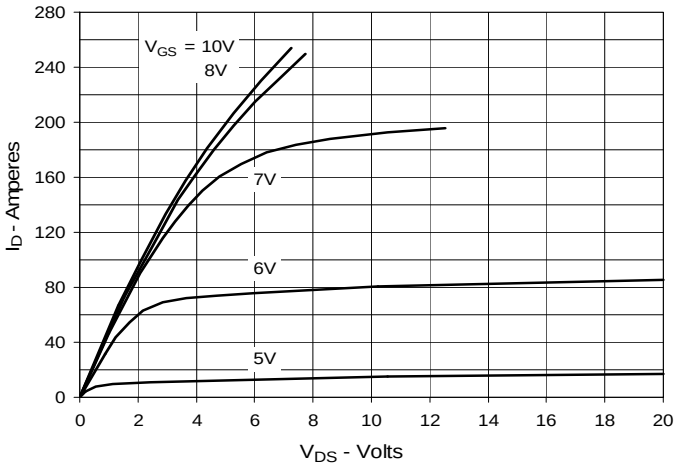


Fig. 3. Output Characteristics @ 125ºC

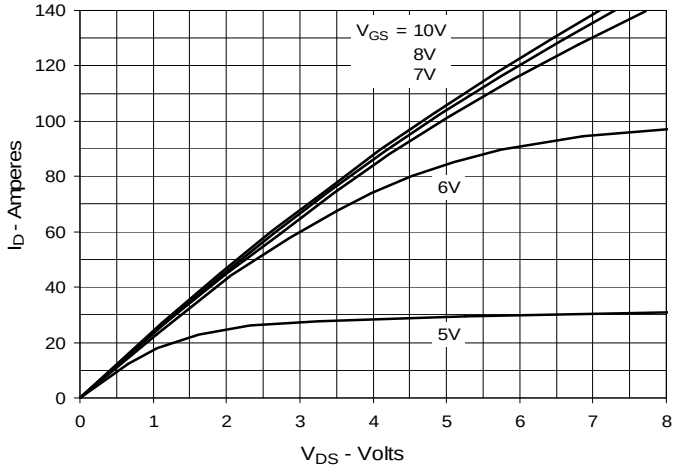


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Junction Temperature

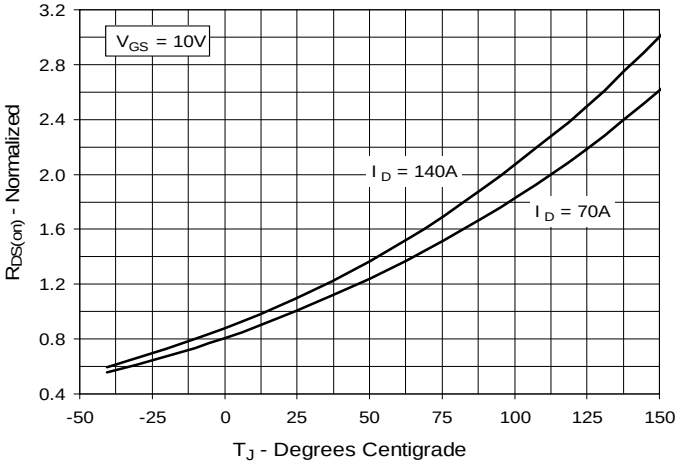


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Drain Current

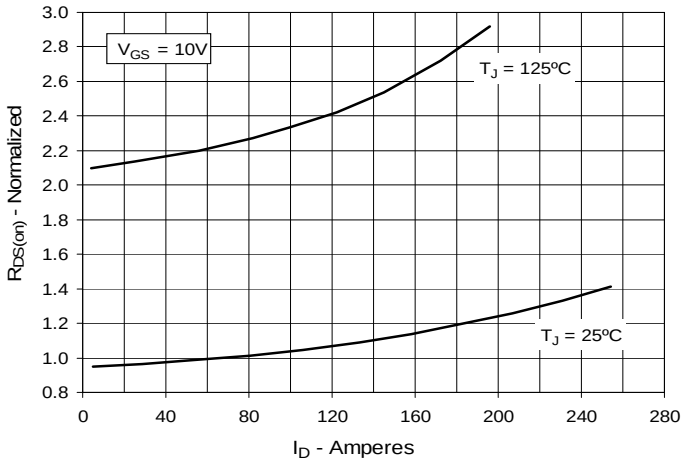


Fig. 6. Maximum Drain Current vs. Case Temperature

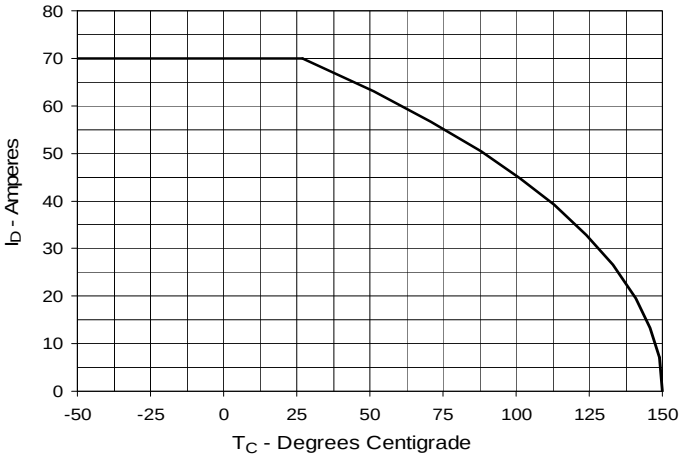


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Fig. 7. Input Admittance

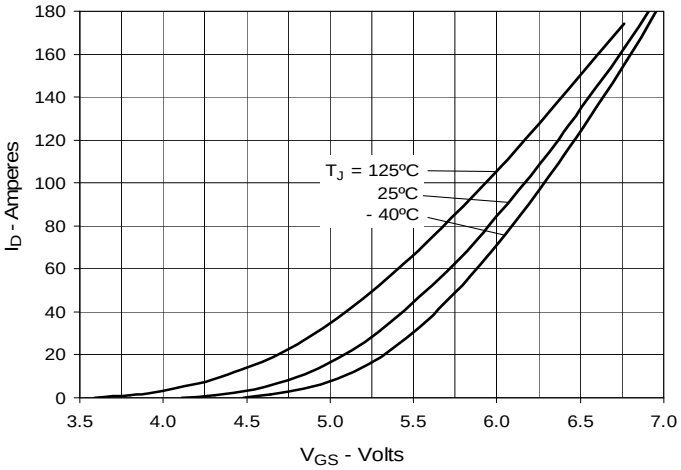

Fig. 8. Transconductance

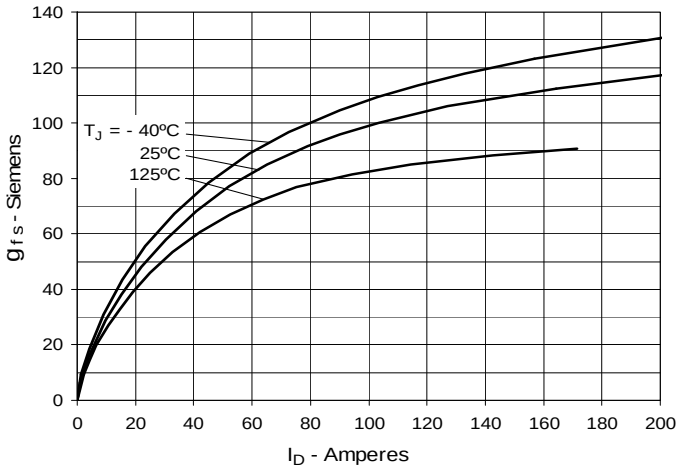

Fig. 9. Forward Voltage Drop of Intrinsic Diode

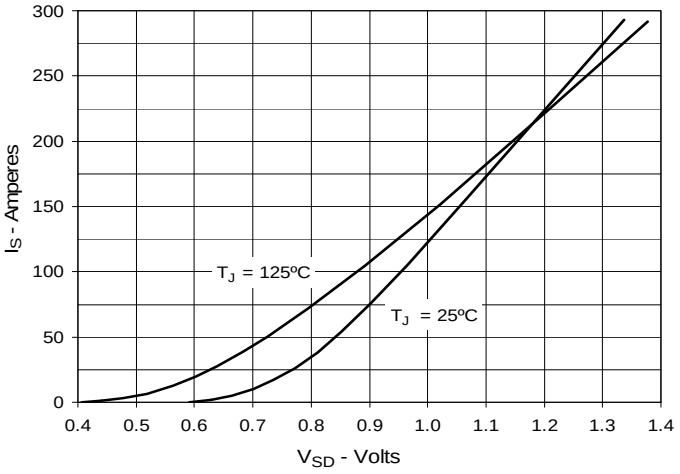

Fig. 10. Gate Charge

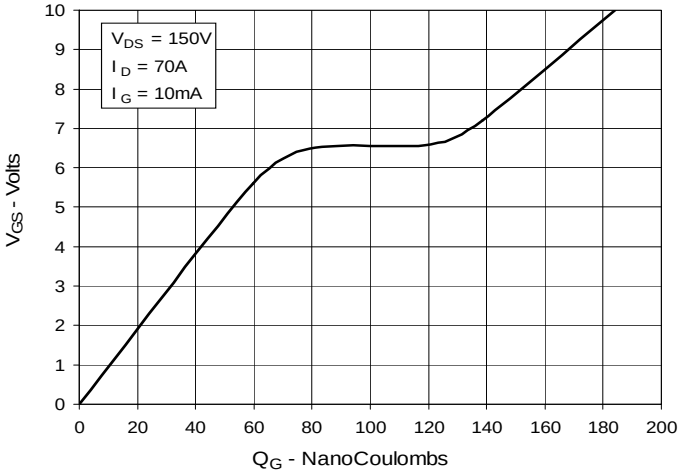

Fig. 11. Capacitance

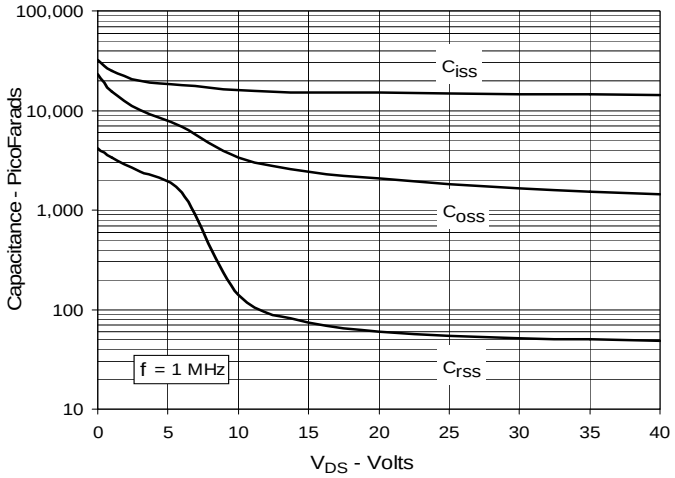

Fig. 12. Forward-Bias Safe Operating Area

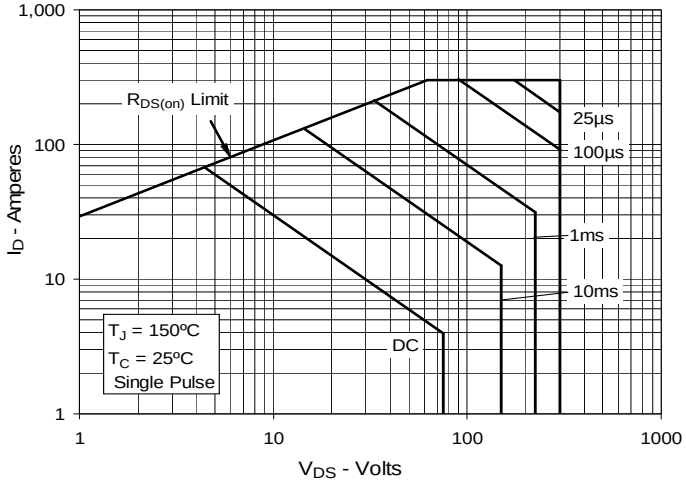

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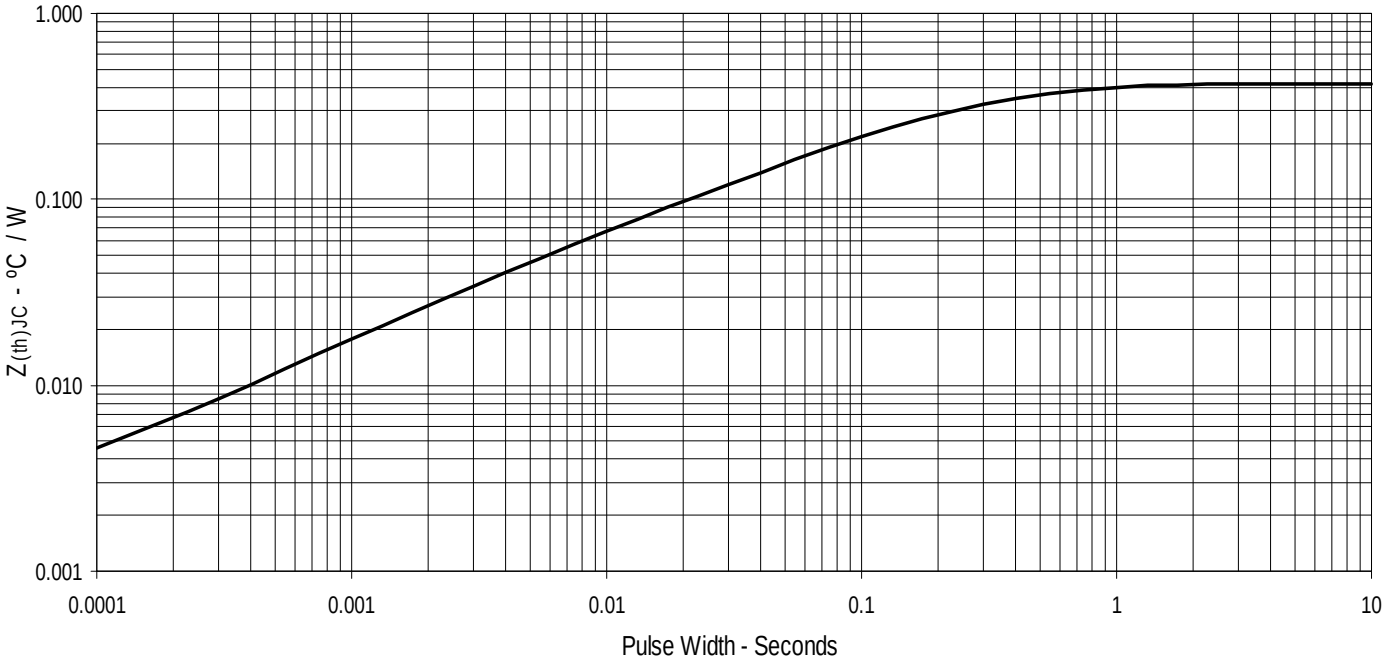
Fig. 13. Maximum Transient Thermal Impedance



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