4-Channel High Current LED Driver with Adaptable Power Control

Data Sheet

ADP8140

FEATURES

- Highly integrated feature set for a high brightness LED driver solution with minimal external components
- 4 current sink channels with an adjustable current from 125 µA to 500 mA
- Analog and pulse-width modulation (PWM) dimming inputs
- Analog and PWM LED current outputs
- 2% (maximum) matching between LED channels
- 5% (maximum) LED current accuracy
- Operates from V_{IN} of 3 V to 30 V; higher voltages easily accomplished with an external Zener diode
- Operates with LED anode supply voltages up to 100 V dc
- Feedback output controls external power source for optimal efficiency and safety
- Multiple ADP8140 IC operation in parallel to control one power supply
- Integrated error amplifier for secondary side control of isolated power supplies
- Easy connection of a temperature thermistor or light sensor
- Provides robust protection of the entire system
  - Power supply overvoltage protection
  - LED overtemperature protection
  - LED short-circuit protection
  - LED open-circuit protection
  - IC overtemperature protection
  - Shorted ISET protection
  - Open ISET and EN protection
- Standby mode for low current consumption
- Fault indicator output
- Small, thermally enhanced, LFCSP package (4 mm × 4 mm)

APPLICATIONS

- High brightness LED lighting
- Large format LED backlighting

TYPICAL APPLICATION CIRCUITS

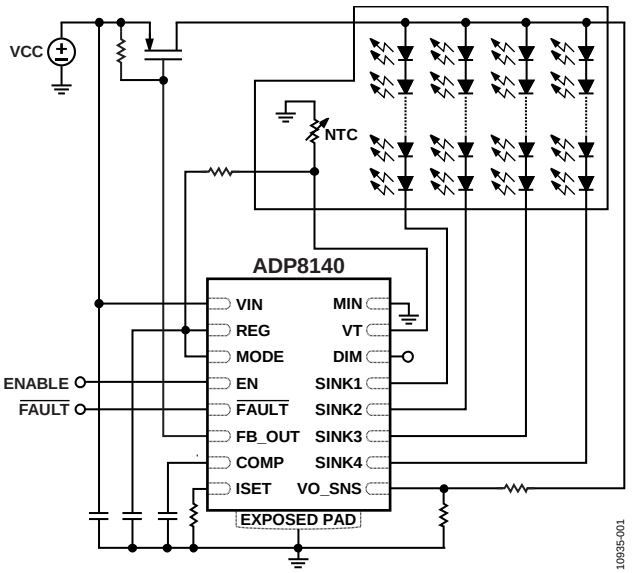

Figure 1. ADP8140 Used with Shunt Regulator

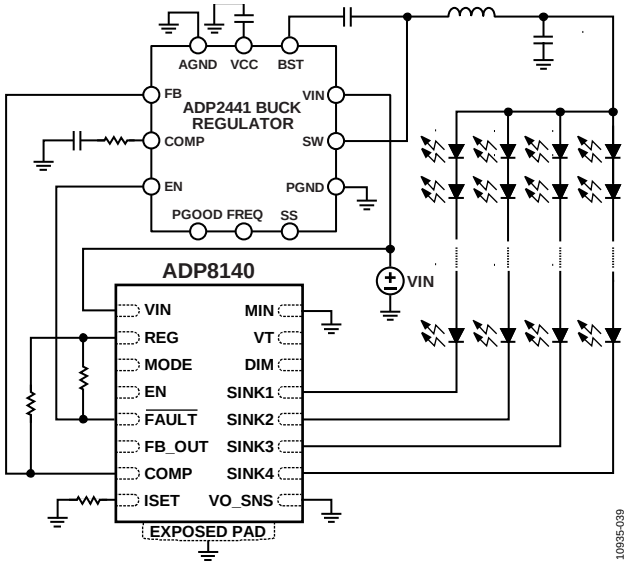

Figure 2. ADP8140 Used with Buck

GENERAL DESCRIPTION

The ADP8140 provides high current control of up to four LED drivers. Each driver can sink up to 500 mA. The sink current is programmed for all four drivers with one external resistor.

The device features a feedback output that controls an external power supply for optimal efficiency. The ADP8140 also protects the LEDs, power supply, and itself against thermal events, short circuits, overvoltages, and LED open circuits. Multiple ADP8140 ICs are easily connected in parallel to drive additional LED strings or higher current LEDs. The ADP8140 is available in a small, thermally enhanced, lead frame chip scale package (LFCSP).

Rev. 0 Document Feedback

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Technical Support www.analog.com

ADP8140* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADP8140: 4 Channel High Current LED Driver with Adaptable Power Control Data Sheet

DESIGN RESOURCES

- ADP8140 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP8140 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

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DOCUMENT FEEDBACK

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REVISION HISTORY

2/15—Revision 0: Initial Version

SPECIFICATIONS

VIN = 12 V, EN = DIM = VT = 3.0 V, MIN = MODE = 0 V. Typical values are at T_J = 25°C and are not guaranteed. Minimum and maximum limits are guaranteed from T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage						
Operating Range	V_{IN}		3.0		30.0	V
Undervoltage Lockout	V_{UVLO}			2.85	2.95	V
Quiescent Current						
During Standby	$I_{Q(STBY)}$	EN = 0 V, VIN = 3.3 V to 30 V		200		µA
During Operation	$I_{Q(ACTIVE)}$	EN = 3 V, VIN = 3.3 V to 30 V, R_{SET} = 71.5 kΩ		4.1	4.5	mA
REG Output						
Output Voltage	V_{REG1}	VIN = 3.3 V to 30 V, I_{REG} = 1 mA	2.85	3.0	3.15	V
	V_{REG2}	VIN = 3 V, I_{REG} = 1 mA	2.85	2.95		V
Source Current	I_{REGMAX}	VIN = 3.3 V to 30 V	15			mA
Load Regulation		VIN = 3.3 V to 30 V, I_{REG} = 0.1 mA to 15 mA		0.75		mV/mA
FEEDBACK OUTPUT						
FB_OUT Error Amplifier (EA) Accuracy	$V_{EA(450)}$		430	450	476	mV
	$V_{EA(350)}$		324	350	380	mV
FB_OUT NMOS Pull-Down Current	I_{FB_PD}	SINKx = 0 V, FB_OUT = 3 V	12.0	15.0	18.0	mA
FB_OUT Stage Gain	G_{FB}	Force 1.2 V and 1.3 V on COMP, measure FB_OUT current (FB_OUT = 12 V)	12500	17000	22000	µmho
FB_OUT Fault Current	I_{FB_FC}	Fault activated, FB_OUT = 30 V		0.04	1	µA
Amplifier Transconductance	$COMP_{GM}$		30	60	120	µmho
Amplifier Transconductance Output						
Source	$COMP_{SOURCE}$	COMP pin output source current		110		µA
Sink	$COMP_{SINK}$	COMP pin output sink current		1.5		mA
Resistance	$COMP_{RO}$			20		MΩ
Low Gain EA	G_{BUFF}	Gain in buffer mode (MODE = 30.1 kΩ to GND)	3.6	3.9	4.2	
Low Gain Bandwidth		MODE = 30.1 kΩ to GND		100		kHz
ISET						
Accuracy	I_{LED_500}	R_{SET} = 5.11 kΩ, SINKx = 600 mV	475	500	525	mA
	I_{LED_350}	R_{SET} = 7.32 kΩ, SINKx = 600 mV	332.5	350	367.5	mA
	I_{LED_100}	R_{SET} = 25.5 kΩ, SINKx = 600 mV	95	100	105	mA
	I_{LED_35}	R_{SET} = 71.5 kΩ, SINKx = 600 mV	33.0	35	37.5	mA
Shorted Current		ISET = GND	500	570	620	mA
Open Current		ISET = open		15	17	mA
CURRENT SINKS						
Current Sink Headroom Voltage at Maximum Current	V_{HR_500}	R_{SET} = 5.11 kΩ, I_{LED} = 95% × I_{LED_500}		320	430	mV
	V_{HR_350}	R_{SET} = 7.32 kΩ, I_{LED} = 95% × I_{LED_350}		210	324	mV
Current at 350 mV	I_{HR_350}	Maximum guaranteed current using the 350 mV reference option	350			mA
Sink Matching		Matching = $(I_{SINK\_MAX} - I_{SINK\_MIN})/(I_{SINK\_MAX} + I_{SINK\_MIN}) \times 100$				
At 500 mA Current	$I_{MATCH500}$			0.2	2	%
At 350 mA Current	$I_{MATCH350}$			0.25	2	%
At 100 mA Current	$I_{MATCH100}$			0.25	2	%
At 35 mA Current	$I_{MATCH35}$			0.3	2	%
SINKx Leakage Current	$I_{SINK(LKG)}$	SINKx pin = 4 V		8	12	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Channel Clamp Threshold						
Low	$V_{CH\_CLMP\_LOW}$	Threshold on SINKx to trigger $V_{CH\_CLMP\_LOW}$, MIN pin = GND	7.4	7.75	8.1	V
High	$V_{CH\_CLMP\_HIGH}$	Threshold on SINKx to trigger $V_{CH\_CLMP\_HIGH}$	14.5	15.1	15.7	V
Channel Clamp Current						
Low	I_{CLMP_LOW}	Channel pull-down current when SINKx > CH_{CLMP_LOW}, R_{SET} = 7.32 kΩ	315	350	385	mA
High	I_{CLMP_HIGH}	Channel pull-down current when SINKx > CH_{CLMP_HIGH}	430	510	600	mA
Channel Clamp Hysteresis	$V_{CH\_CLMP\_HYS}$	Hysteresis after either channel clamp is triggered		1.2		V
Lowest SINKx Current		Output current for DIM = 0 V and R_{SET} = 10 kΩ (see Figure 15)		125		µA
INPUT CONTROLS						
Input Threshold (Low)	V_{IL}				0.6	V
Input Threshold (High)	V_{IH}		1.1			V
EN Input Resistance	R_{EN}	EN = 1.2 V		400		kΩ
MODE Pin Pull-Up Current	I_M		15	20	24	µA
MODE Threshold 1, 30.1 kΩ	V_{M1}	Threshold for increasing mode voltage to enter dc buffer operation	0.35	0.4	0.45	V
MODE Threshold 2, 52.3 kΩ	V_{M2}	Threshold for increasing mode voltage to enter PWM buffer operation	0.75	0.8	0.85	V
MODE Threshold 3	V_{M3}	Threshold for increasing mode voltage to enter PWM EA operation	1.25	1.3	1.35	V
LED Scaling Controls						
DIM and VT Limit Voltage	VT_{LIMIT}	VT (and DIM if MODE = GND) voltage to produce 100% output current	1.9	2.0	2.1	V
Dimming Accuracy	I_{LED_DIM1}	I_{LED_DIM1}/I_{LED_100}, VT = 1 V, MIN = 0 V, R_{SET} = 25.5 kΩ	48	50	52	%
	I_{LED_DIM2}	I_{LED_DIM2}/I_{LED_100}, DIM = 0.2 V, MODE = GND, R_{SET} = 25.5 kΩ	9.4	10	10.4	%
	I_{LED_DIM3}	I_{LED_DIM3}/I_{LED_100}, DIM = 50%,140 Hz, MODE = REG, R_{SET} = 25.5 kΩ	48	50	52	%
VT Pull-Up Current Source				0.6	1	µA
DIM Pin Frequency Range		MODE = REG	0.14		40	kHz
MIN Comparator Hysteresis	V_{MIN_HYS}			55		mV
MIN Pin PWM Mode Threshold	V_{MIN_PWM}	Voltage on MIN pin at which VT changes from scaling LED current to pulsing LED current	2.2	2.3	2.4	V
PWM Delay and Rise/Fall Time		Delay from VT low to high (or high to low) to LED current low to high (or high to low), MIN = REG		20		µs
THERMAL FOLDBACK (INTERNAL)						
Thermal Foldback Threshold	TFB_{THRES}			135		°C
Thermal Shutdown Threshold	TSD_{THRES}			150		°C
Thermal Shutdown Hysteresis	TSD_{HYS}			20		°C
FAULT DETECTION						
$\overline{FAULT}$ Threshold	V_{FAULT_TH}	Threshold for $\overline{FAULT}$ comparator	1.14	1.2	1.26	V
$\overline{FAULT}$ Hysteresis	V_{FAULT_HYS}	Hysteresis for $\overline{FAULT}$ comparator		100		mV
$\overline{FAULT}$ Filter	t_{FAULT}	VO_SNS and $\overline{FAULT}$ shutdown noise filter		10		µs
$\overline{FAULT}$ Pull-Down Resistance	$\overline{FAULT}_{PD}$	Fault activated	7	15	20	Ω
VO_SNS						
Threshold	$V_{VO\_SNS\_TH}$	Threshold for VO_SNS comparator	1.176	1.2	1.224	V
Hysteresis	$V_{VO\_SNS\_HYS}$	Hysteresis for VO_SNS comparator		50		mV
Leakage Current	I_{VO_SNS}				50	nA
Open SINKx Fault Threshold	V_{SFD_OPEN}	SINKx pin voltage threshold to remove a sink from the feedback loop after a VOUT_OVP fault		80		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Channel Overvoltage Threshold	V_{CH_OVP}	Threshold on SINKx to trigger CH_OVP fault	5.3	5.7	6.1	V
Channel Overvoltage Hysteresis	$V_{CH\_OVP\_HYS}$	Hysteresis after V_{CH_OVP} is triggered		1.2		V
Short SINKx Fault Threshold	V_{SFD_SHORT}	SINKx pin voltage threshold to remove a sink from the feedback loop after a CH_OVP fault		525		mV

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, FB_OUT to GND	−0.3 V to +31 V
SINKx to GND	−0.3 V to +21 V
MODE, COMP, REG, MIN, DIM, VT, ISET to GND	−0.3 V to +3.6 V
EN, $\overline{\text{FAULT}}$, VO_SNS to GND	−0.3 V to +6.0 V
Operating Ambient Temperature Range	−40°C to +105°C[1]
Operating Junction Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−45°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD (Electrostatic Discharge)	
Human Body Model (HBM)	±1.5 kV
Charged Device Model (CDM)	±500 V

[1] The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). See the Maximum Temperature Ranges section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

MAXIMUM TEMPERATURE RANGES

The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). Therefore, in situations where the ADP8140 is exposed to poor thermal resistance and a high power dissipation (P_D), the maximum ambient temperature may need to be derated. In these cases, the ambient temperature maximum can be calculated with the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - (\theta_{JA} \times P_{D(MAX)})$$

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA}, θ_{JB} (junction to board), and θ_{JC} (junction to case) are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling. The LFCSP exposed pad must be soldered to GND.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
16-Lead LFCSP	33.2	12.4	2.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

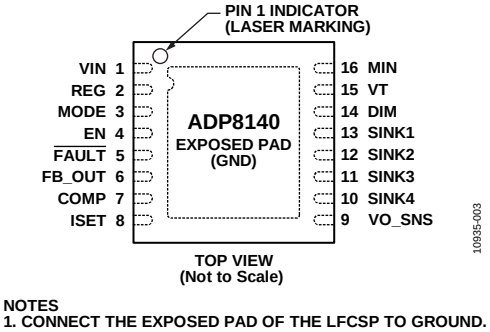

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Supply Voltage Input (3.0 V to 30 V).
2	REG	Regulated 3.0 V (Typical) Source. Connect a 1.0 µF (or greater) capacitor from REG to ground.
3	MODE	Operation Mode. If MODE is connected to ground, the device is placed in dc EA operation. If MODE is connected to REG, the device is placed in PWM EA operation. If MODE is connected via a 30.1 kΩ resistor to ground, the device is placed in dc low gain buffer operation. If MODE is connected via a 52.3 kΩ resistor to ground, the device is placed in PWM low gain buffer operation. The MODE pin is read only once at power-up (when VIN exceeds 3 V). Any changes to the MODE pin after applying power are ignored. See the MODE Pin Operation section for more information.
4	EN	Enable Input. Pull high (above $V_{IH(MIN)}$) to enable the device. EN is internally pulled low with a 400 kΩ (typical) resistor.
5	$\overline{\text{FAULT}}$	Fault Output. This pin must be connected to an external pull-up resistor. If using multiple ADP8140 ICs in parallel, all $\overline{\text{FAULT}}$ pins must be connected together.
6	FB_OUT	Feedback Output. The FB_OUT pin is a control signal for the external power stage. The action of this pin depends on the MODE setting.
7	COMP	Compensation Pin for EA. The COMP pin is a control signal for the external power stage. COMP is a dual function pin. The action of this pin depends on the MODE setting.
8	ISET	Output Current Setting. Connect a resistor to ground to set the output current. If left floating, the current sinks are set to 15 mA.
9	VO_SNS	Overvoltage Protection Sensing Input. Connect the VO_SNS pin through a resistor divider to the top of the LED strings, or connect it to ground to disable overvoltage sensing.
10	SINK4	Current Sink for LED Channel 4.
11	SINK3	Current Sink for LED Channel 3.
12	SINK2	Current Sink for LED Channel 2.
13	SINK1	Current Sink for LED Channel 1.
14	DIM	Dim Input. The DIM pin scales the LED current from the PWM signal or dc voltage. The action of this pin depends on the MODE setting.
15	VT	Voltage Threshold. VT is a dual function pin. If MIN < 2.2 V at startup, VT is an analog current reduction pin. A voltage on VT scales the LED current. If MIN is connected to REG at startup, a PWM signal applied to VT pulses the LED current.
16	MIN	Minimum Voltage Threshold. If MIN < 2.2 V at startup, the MIN voltage sets the minimum voltage threshold for the VT pin. VT voltages below the MIN voltage shuts down the power stage. If MIN is connected to REG at startup, a PWM signal applied to VT pulses the LED current.
	EPAD (GND)	Exposed Pad (Ground). Connect the exposed pad of the LFCSP to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12 V, EN = DIM = VT = 3.0 V, MIN = MODE = 0 V, V_{SINKx} = 450 mV, T_A = 25°C, unless otherwise noted.

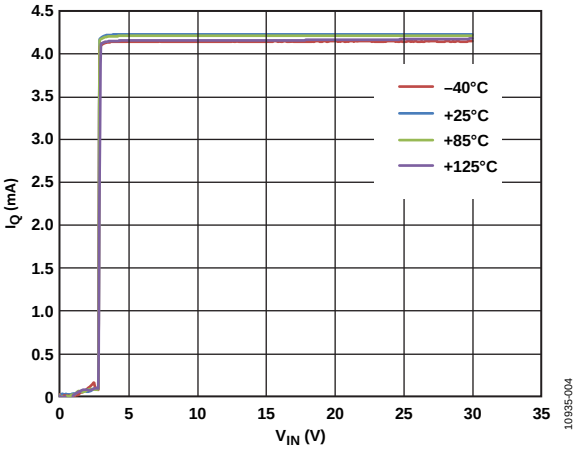

Figure 4. Typical Operating Current vs. V_{IN}, EN = 3 V, R_{SET} = 71.5 kΩ

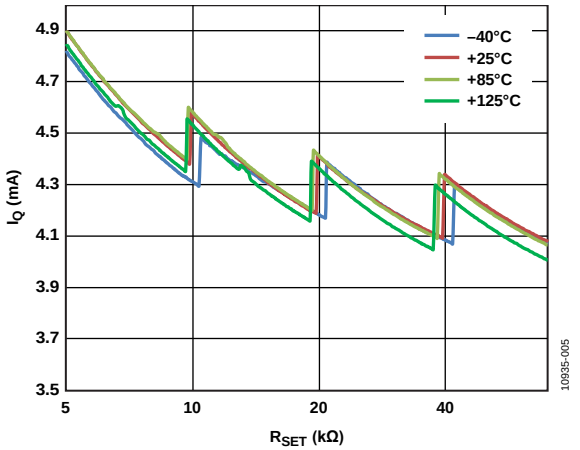

Figure 5. Typical Operating Current vs. R_{SET}

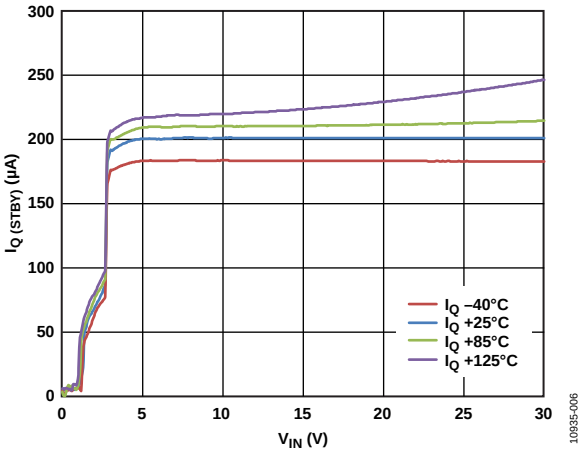

Figure 6. Typical Standby Current vs. V_{IN}, EN = 0 V

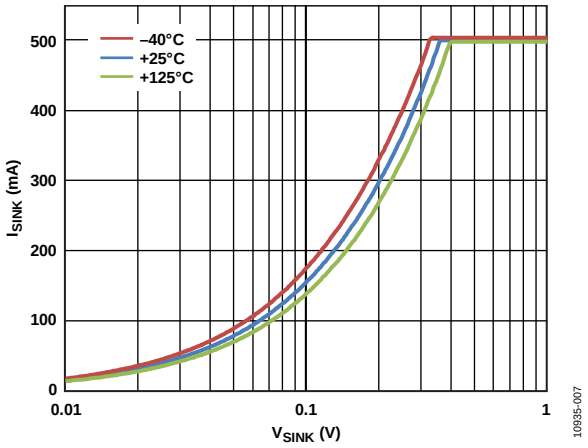

Figure 7. Typical Sink Current vs. Sink Voltage, R_{SET} = 5.11 kΩ

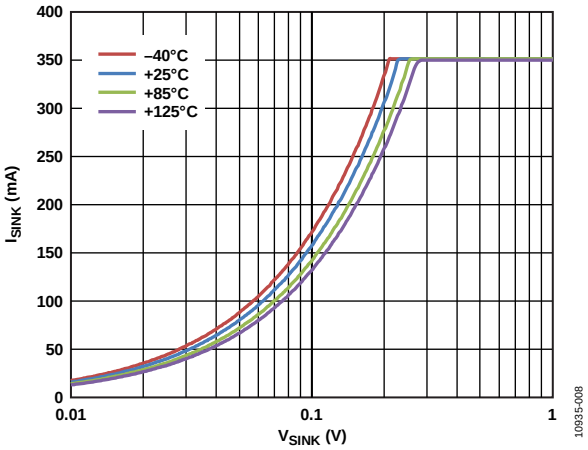

Figure 8. Typical Sink Current vs. Sink Voltage, R_{SET} = 7.32 kΩ

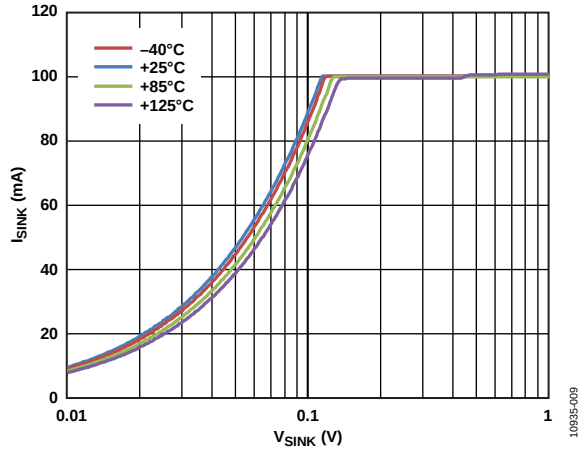

Figure 9. Typical Sink Current vs. Sink Voltage, R_{SET} = 25.5 kΩ

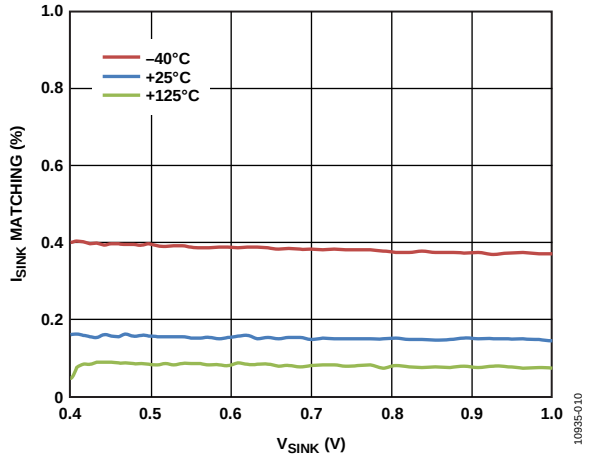

Figure 10. Typical Sink Current Matching vs. Sink Voltage, R_{SET} = 5.11 kΩ

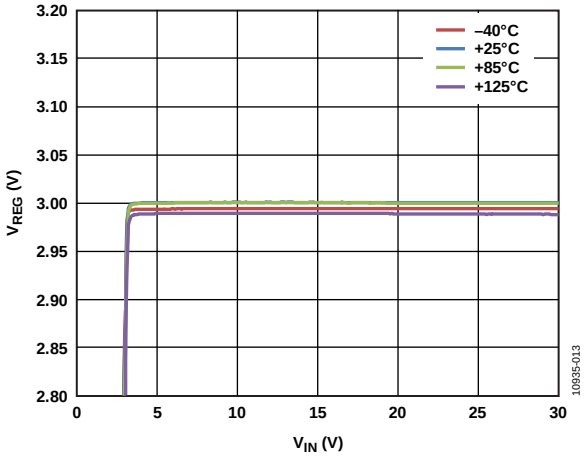

Figure 13. REG Voltage vs. Input Voltage

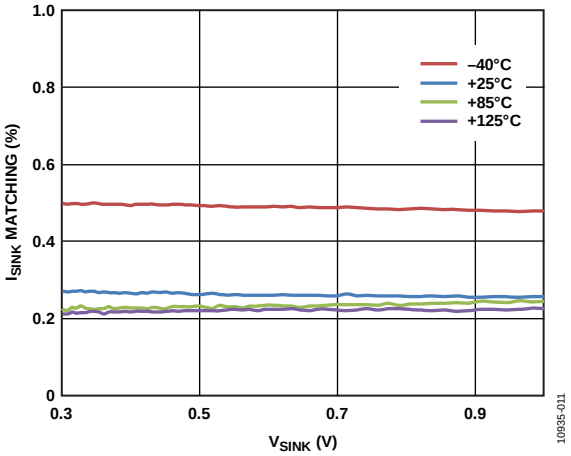

Figure 11. Typical Sink Current Matching vs. Sink Voltage, R_{SET} = 7.32 kΩ

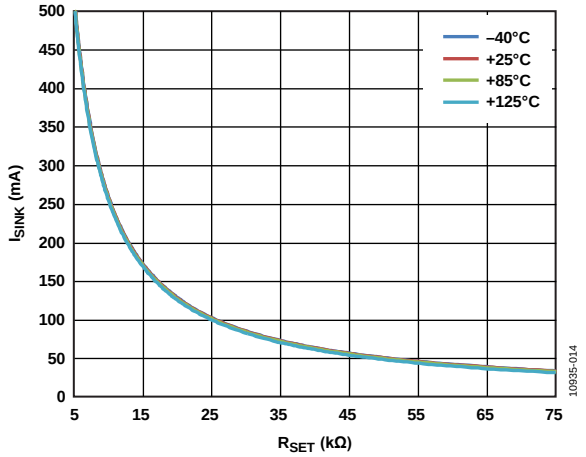

Figure 14. Sink Current vs. R_{SET} (DIM = 3 V)

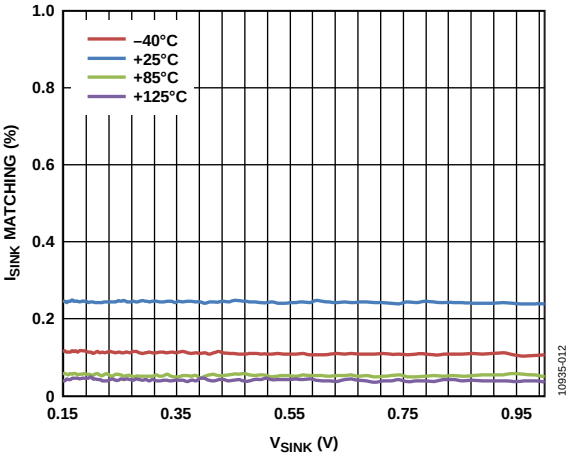

Figure 12. Typical Sink Current Matching vs. Sink Voltage, R_{SET} = 25.5 kΩ

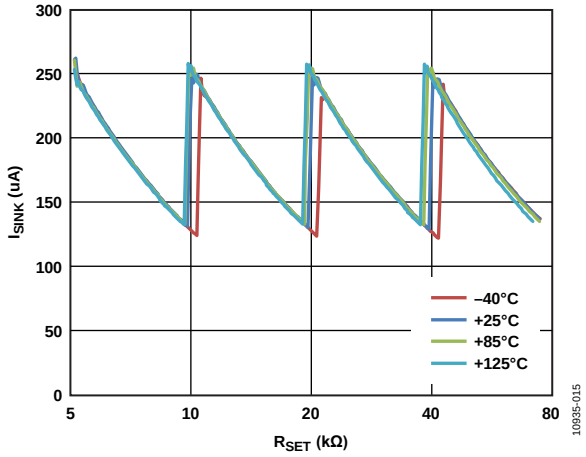

Figure 15. Sink Current vs. R_{SET} (DIM = 0 V)

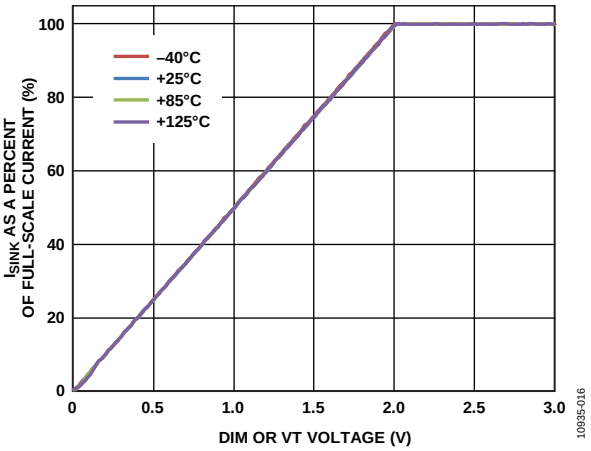

Figure 16. Typical Sink Current vs. DIM or VT Voltage (MODE = 0, MIN = 0 V)

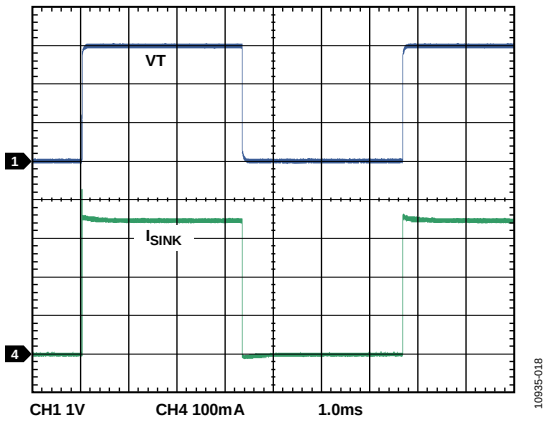

Figure 18. Typical Sink Current Waveforms with PWM on VT Pin (MIN = 3 V)

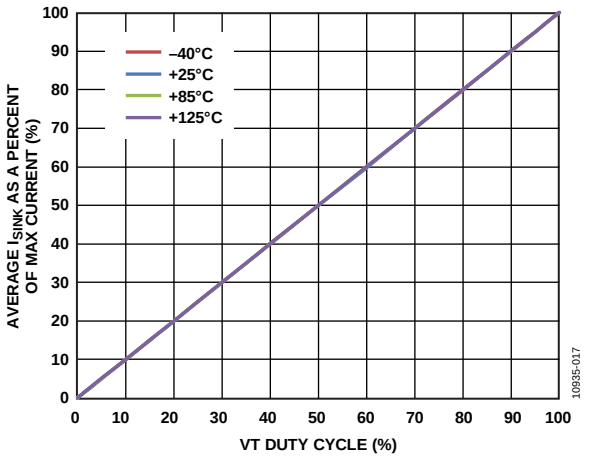

Figure 17. Typical Average Sink Current vs. VT Duty Cycle (MIN = 3 V, VT Frequency = 120 Hz)

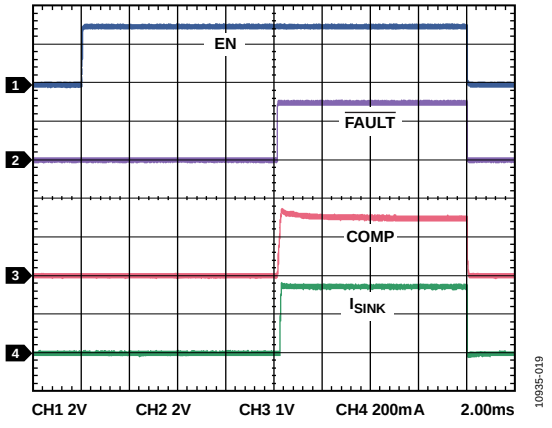

Figure 19. Start-Up Sequence (See Figure 1 Setup)

THEORY OF OPERATION

The ADP8140 provides high current control of up to four LED channels. Each driver can sink up to 500 mA. One external resistor programs the sink current for all four channels. The device features a feedback output that controls an external power supply for optimal efficiency. The ADP8140 also protects the LEDs, power supply, and itself against thermal events, short circuits, and LED open circuits. Multiple ADP8140 ICs are easily connected in parallel to drive additional LED strings or higher current LEDs.

START-UP SEQUENCE

To start the ADP8140, VIN must be applied in excess of the UVLO threshold and the EN pin must be high. However, even with EN low, the REG pin produces a constant 3.0 V (typical) on its output. REG can be used as a low current supply, as needed. In this operation, with EN low, the ADP8140 consumes no more than 200 µA (typical). A 400 kΩ (typical) resistor from EN to GND ensures that the ADP8140 is shut down in the event of an open connection on the EN pin.

When EN also goes high, the power stage starts up and the current sinks are enabled. There is an approximate 8 ms delay after EN goes high. When the sinks are enabled, the $\overline{\text{FAULT}}$ pin is released and the COMP and FB_OUT pins begin their normal regulation. When EN goes low, the SINKx pins are left on for another 100 µs to discharge any voltage from the power stage output. The device then enters low current consumption operation.

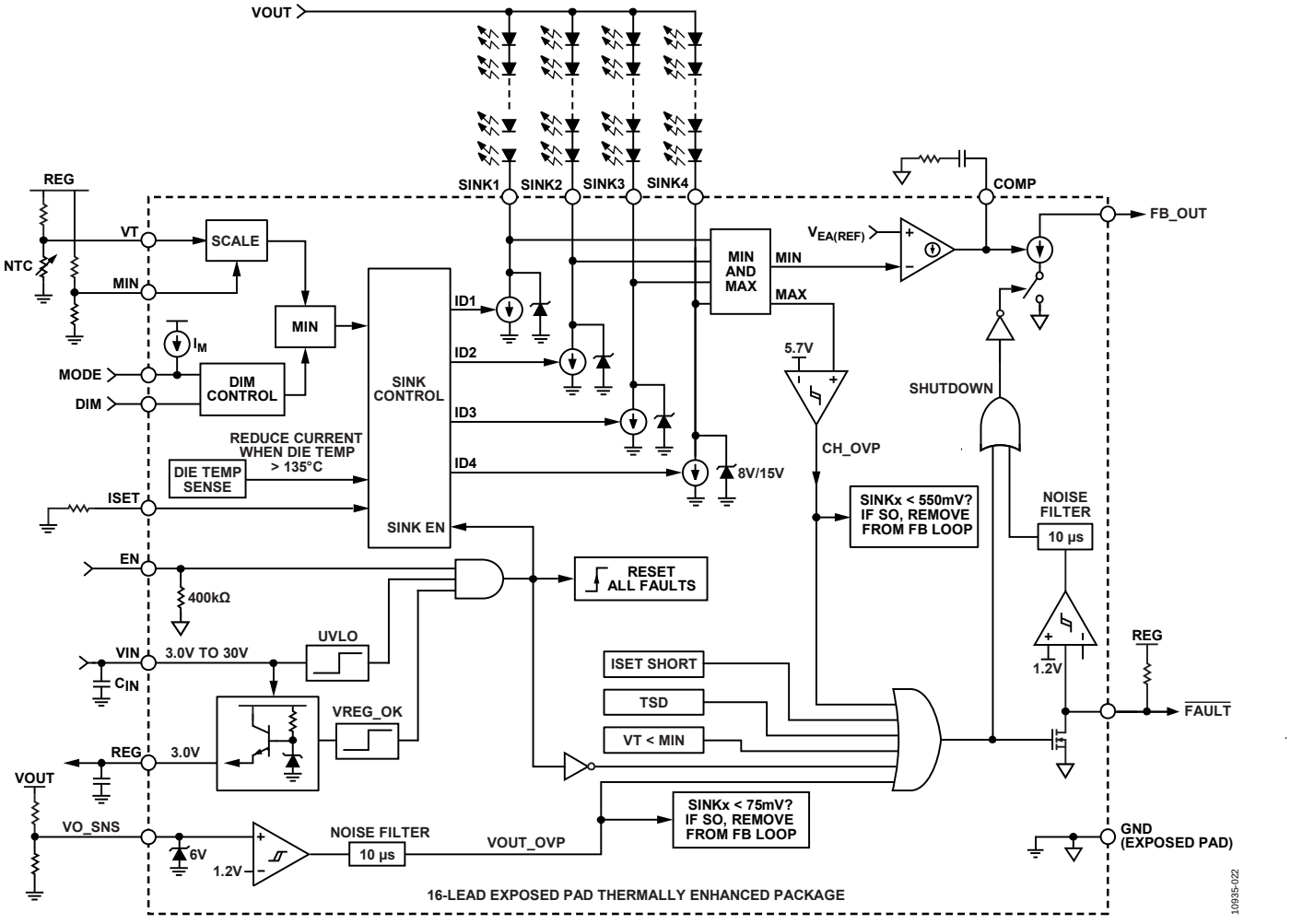

Figure 20. Detailed Block Diagram

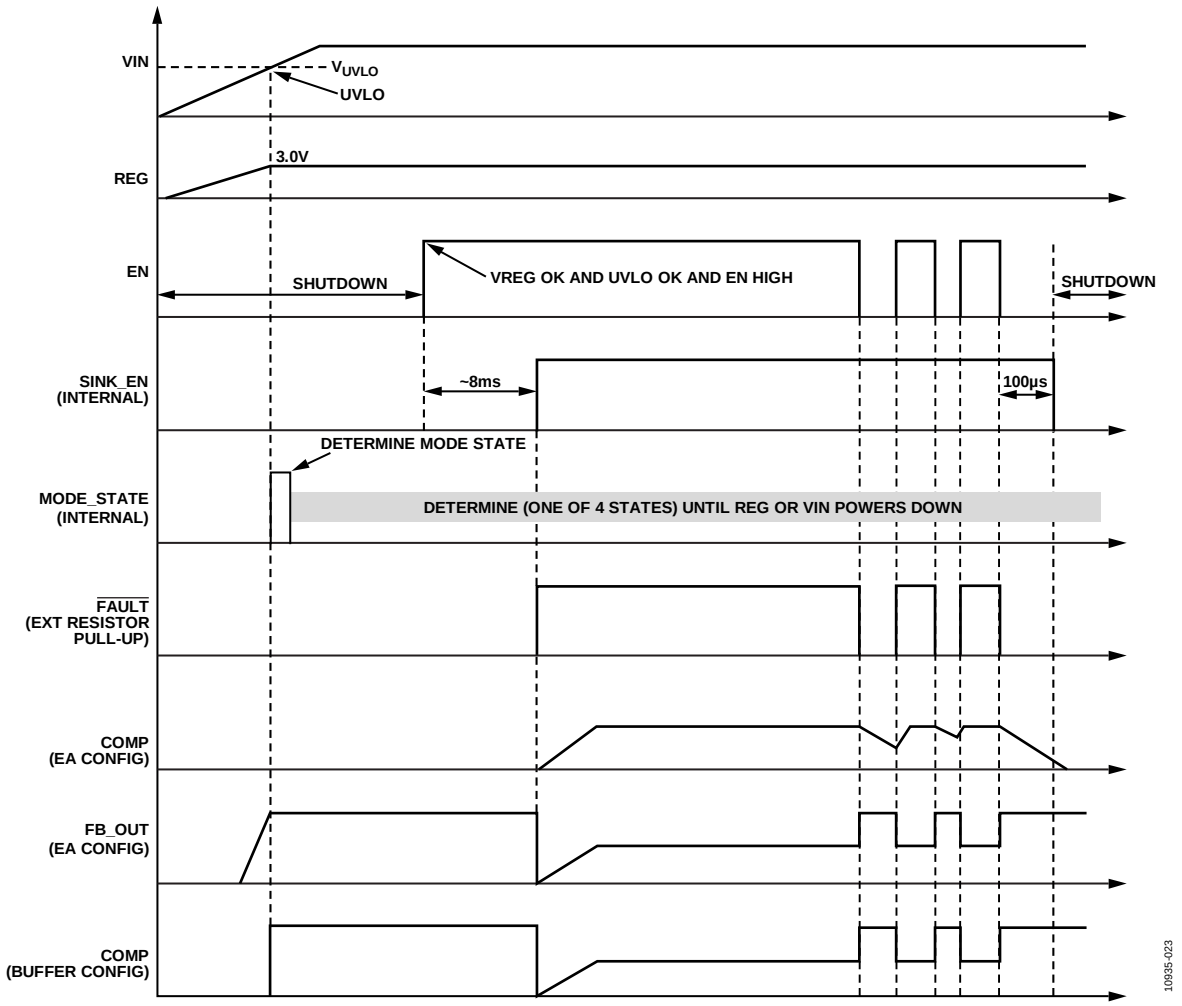

Figure 21. Start-Up Timing and Signals

CURRENT SINKS

The ADP8140 contains four internal current sinks. Each current sink is capable of delivering 125 µA to 500 mA. To ensure accurate regulation, the voltage on the current sinks must be greater than the maximum headroom voltage given in Table 1. For additional information on the headroom voltage, see Figure 7 to Figure 9. All current sinks have their maximum current set by the external resistor, R_{SET}. To determine the value of R_{SET}, use Equation 1. A graph of sink current vs. R_{SET} is shown in Figure 14.

$$R_{SET}(\text{k}\Omega) = \frac{2560}{I_{SINK}(\text{mA})} \quad (1)$$

Multiple sinks can be combined together for higher currents per LED string. For example, two sinks can be shorted together to drive two strings of LEDs, each at up to 1 A, or four sinks combined to drive one string of LEDs at up to 2.0 A.

A resistor must always be connected to the ISET pin. However, in the event that ISET is accidentally left open, the ADP8140 defaults to a typical current of 15 mA (typical) per sink. If ISET is accidentally shorted to GND, the ADP8140 limits the current per sink to 570 mA (typical) and shuts down the power stage ($\overline{\text{FAULT}}$ goes low and FB_OUT and COMP are disabled).

Each current sink has a maximum rated voltage of 20 V. However, the maximum output voltage driving all the current sinks, through the LEDs, is allowed to exceed 20 V. The LEDs drop enough voltage so that the SINKx voltage remains close to the FB_OUT EA accuracy value, $V_{EA(REF)}$ (where REF is the reference voltage). Because the ADP8140 controls the power stage, the voltage is not present when off or during a fault. Therefore, the ADP8140 can be safely used in conjunction with power supplies that produce over 100 V for their output.

POWER CONTROL OPERATION

The ADP8140 controls a power stage with its COMP and FB_OUT pins. The power stage allows the IC to optimize the efficiency and protection of the LEDs. The ADP8140 operates in two power control modes: error amplifier and low gain buffer. The MODE pin is used to select the power control mode.

MODE PIN OPERATION

The MODE pin is used to program one of four possible modes of operation. The condition of the MODE pin affects the DIM pin input (see the Reducing the LED Current with the DIM Pin section) and the power control mode (see Power Control Modes section). The MODE pin state is read at power-up only, when VIN crosses the UVLO threshold. After this point, the MODE pin voltage is 0 V. The MODE status cannot change after power-up.

Table 5. Modes of Operation Programmed by the MODE Pin

MODE Connection	DIM Pin Mode	Power Control
GND	Analog voltage	Error amplifier
30.1 kΩ to GND	Analog voltage	Low gain buffer
52.3 kΩ to GND	PWM signal	Low gain buffer
REG	PWM signal	Error amplifier

POWER CONTROL MODES

Error Amplifier Power Control

In the error amplifier power control mode, the ADP8140 applies the minimum voltage of the four current sinks to the inverting input of an internal error amplifier. The output of this error amplifier connects to the FB_OUT inverting buffer.

The FB_OUT pin outputs a current, which indicates power control. A higher FB_OUT sink current indicates that more power is required to the LEDs. A lower FB_OUT sink current indicates that less power is required for the LEDs. This operation makes the FB_OUT ideal for any power control application that does not normally have an error amplifier. The two primary applications for this are as follows:

- Controlling an optocoupler on the secondary side of an isolated power supply
- Controlling a PMOS transistor to regulate power in a fixed output voltage supply.

Depending on the power stage used, an RC network must be connected to the COMP pin. The COMP pin connects to the output of the FB_OUT transconductance amplifier. To select the COMP resistor and capacitor values, a free simulation tool, ADIsimPE, is available at: www.analog.com/ADIsimPE.

Using this tool, and the included ADP8140 circuit model, the loop control and stability can be easily simulated and adjusted for different setups.

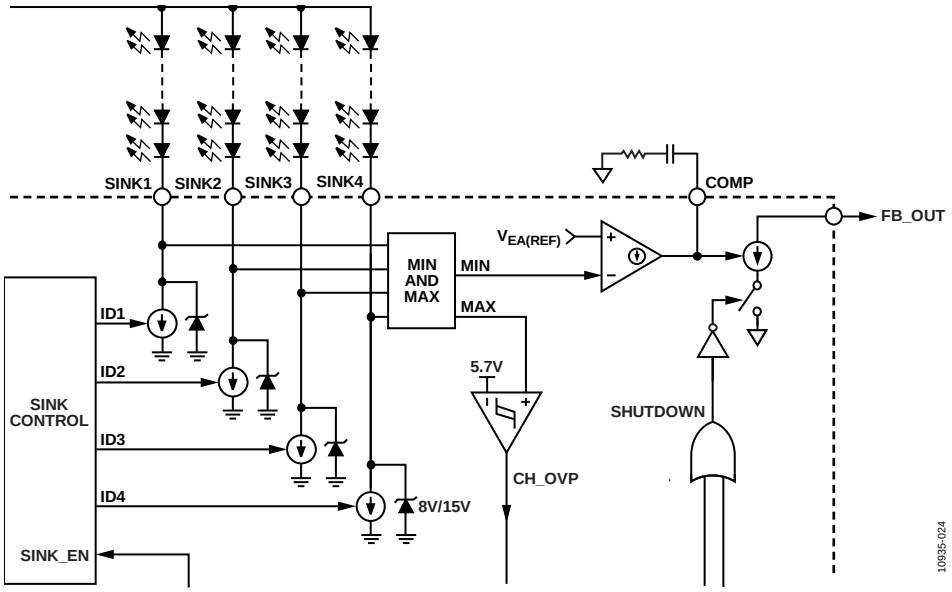

Figure 22. Error Amplifier Power Control

Low Gain Buffer Power Control

In the low gain buffer power control mode, the ADP8140 multiplies the minimum voltage of the four current sinks by G_{BUFF} (3.9 typical; see Table 1) and outputs it to the COMP pin. This mode allows the ADP8140 to easily control nearly any switched mode power supply (SMPS) control IC, such as a buck regulator or boost controller. Common examples are shown in Figure 32 to Figure 36.

In this mode, the COMP pin is connected to the feedback (FB) input of an SMPS controller. The FB_OUT pin can be left floating or connected to GND. Do not tie it to COMP or any other pin. Connect the $\overline{\text{FAULT}}$ pin to the EN signal of the SMPS IC. This connection ensures that the power delivery immediately shuts down in the event of a fault.

The values of R1, R2, and R3 program the minimum headroom voltage on the SINKx pins and set the maximum voltage that the SMPS FB input receives. A spreadsheet is available at www.analog.com/ADP8140 to assist in these calculations. Otherwise, to find the values start with the following equation:

$$R2 = R1 \times \left(\frac{3.9 \times V_{HR}}{FB\_REF} - 1 \right)$$

where:

FB_REF is the internal error amplifier reference voltage of the SMPS IC. This is typically 600 mV or 1.2 V. However, it does vary for different ICs; therefore, consult the data sheet of that IC.

V_{HR} is the minimum headroom voltage that the ADP8140 current sinks need (see Figure 7 to Figure 9). This value varies based on the maximum sink current that is programmed on the ISET pin.

Set the value of R1 to be small enough so that the internal 250 kΩ pull-down resistance on the COMP pin does not affect the total resistance. For example, if R1 = 10 kΩ, V_{HR} = 325 mV, and FB_REF = 600 mV, then

$$R2 = 10\ \text{k}\Omega \times \left(\frac{3.9 \times 0.325}{0.6} - 1 \right) = 11.1\ \text{k}\Omega$$

Next, select R3 to set the maximum voltage applied to the SMPS FB input.

$$R3 = \frac{V_{REG} \times R1}{FB_{MAX}} - R1 - R2$$

where FB_{MAX} is the maximum voltage desired on the SMPS FB input. Therefore, if FB_{MAX} = 720 mV,

$$R3 = \frac{3\ \text{V} \times 10\ \text{k}\Omega}{0.720} - 10\ \text{k}\Omega - 11.1\ \text{k}\Omega = 20.6\ \text{k}\Omega$$

Ensure that FB_{MAX} is sufficiently higher than the maximum FB_REF operating point. Some extra margin is beneficial.

DIMMING THE LED CURRENT

The ADP8140 offers multiple methods of dimming. The dimming input can be either an analog voltage or a PWM signal. The LED output current can be either scaled (dc dimming) or pulsed on and off in response to the PWM input signal. The two dimming pins, DIM and VT, provides different functions, but both pins can be used for dimming simultaneously, which provides enormous flexibility in controlling the LED current.

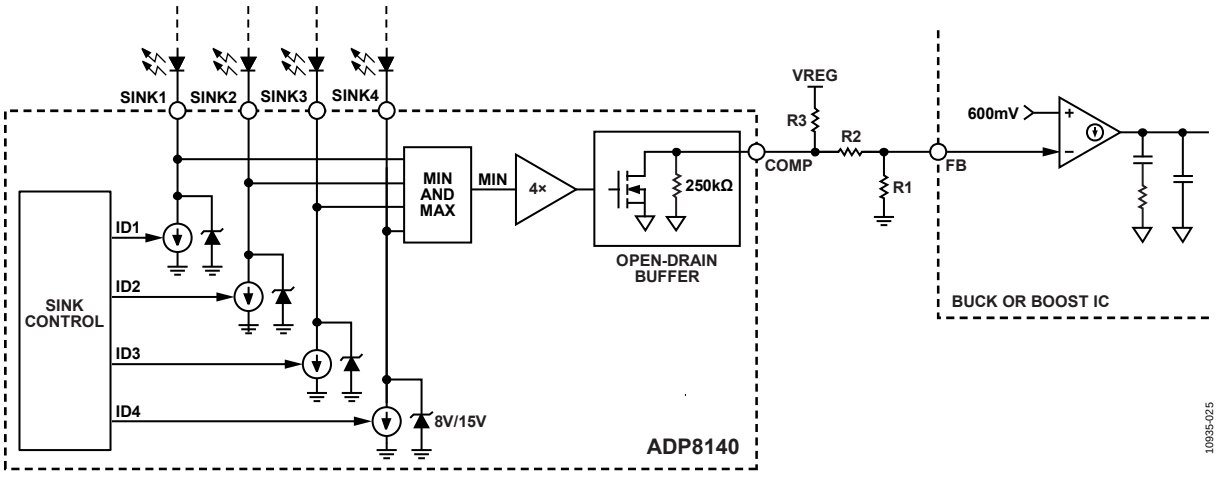

Figure 23. Low Gain Buffer Power Control

REDUCING THE LED CURRENT WITH THE DIM PIN

The DIM pin scales the output current when either an analog voltage or a PWM signal is applied to it. The response of the ADP8140 to the DIM pin depends on the condition of the MODE pin.

If the MODE pin is connected to GND or a 30.1 kΩ resistor at startup, the DIM pin functions as an analog voltage input. As such, a DIM voltage of 2 V or greater does not impact the output current. A DIM voltage of 0 V reduces the output current to as low as 125 µA (see Figure 15). Any DIM voltage between 0 V and 2 V linearly scales the output current.

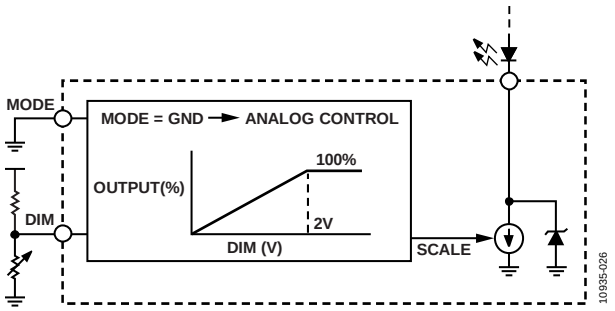

Figure 24. Reducing the Output Current by Applying an Analog Voltage to the DIM Pin

If MODE is connected to REG or to a 52.3 kΩ resistor at startup, a PWM duty cycle applied to the DIM pin is internally filtered and used to scale the output currents. Set the DIM pin frequency between 140 Hz and 40 kHz. A lower frequency PWM signal gives the ADP8140 more information about the applied duty cycle and leads to better resolution of the duty cycle, which translates into smaller LED current step sizes on the current sink digital-to-analog converters (DACs).

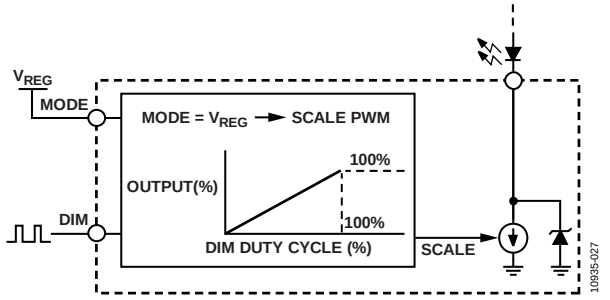

Figure 25. Reducing the Average Output Current by Pulse Width Modulating the Current Sinks with the DIM Pin

When DIM = 0 V, or 0% duty cycle, the minimum output current is a function of the programmed R_{SET} value. This minimum value varies between 125 µA and 250 µA, depending on the R_{SET} value. The typical value as a function of R_{SET} is shown in Figure 15 of the Typical Performance Characteristics section.

DIMMING LEDS WITH THE VT PIN

The VT pin has two modes of operation, depending on the configuration of the MIN pin.

If MIN is connected to REG at startup, a PWM input to the VT pin pulses the LED current sinks. If the PWM input is high, the current goes to the value dictated by the ISET and DIM pins. If the PWM input is low, the current becomes the minimum current as defined in Figure 15. This small current allows the LEDs to be slightly biased and minimizes the voltage difference between the off and on states, which greatly reduces the response time of the power delivery loop.

In this mode, the 7.75 V SINKx clamp is disabled. When the clamp is disabled, the voltages on the SINKx pins rise as high as 15.1 V (typical) during the LED off time.

If MIN < 2.2 V, the voltage on the VT pin linearly scales the LED current. VT voltages greater than 2 V (typical) produce 100% of the programmed ISET current. When VT is less than 2 V, the output current is reduced 1% per 20 mV. If the voltage on the VT pin is below the voltage on the MIN pin, the power supply to the LEDs is disabled. If the VT pin voltage rises above the MIN threshold, plus some hysteresis, the power supply is reenabled. If both the VT pin and the DIM pin are used for analog dimming, the pin that gives the lower LED current is used to set the LED current.

To implement thermal protection of the LEDs, the VT pin is connected to an external negative temperature coefficient (NTC) resistor. This NTC resistor is typically placed on the LED heat sink. Selecting the value of the NTC and the resistor in the network shapes the slope of the VT voltage in response to the LED temperature. A resistor divider on the MIN pin sets the level at which the power stage (FB_OUT and COMP) are disabled.

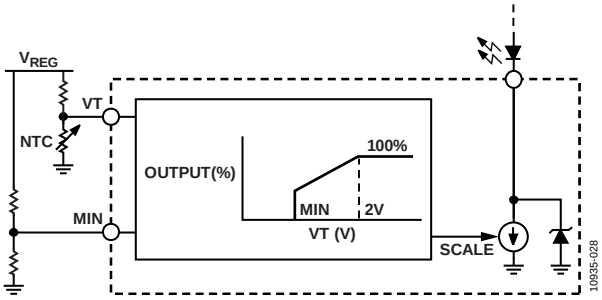

Figure 26. Using an External NTC to Implement LED Thermal Protection

FAULT PROTECTIONS

To ensure the safety of the LEDs, the ADP8140 IC, and the power source, the ADP8140 includes a comprehensive array of detection and protection features.

- Power supply overvoltage protection
- LED overtemperature protection
- LED short-circuit protection
- LED open-circuit protection
- IC overtemperature protection
- Shorted ISET protection
- Open ISET and EN protection

These features are summarized in the flowchart shown in Figure 27.

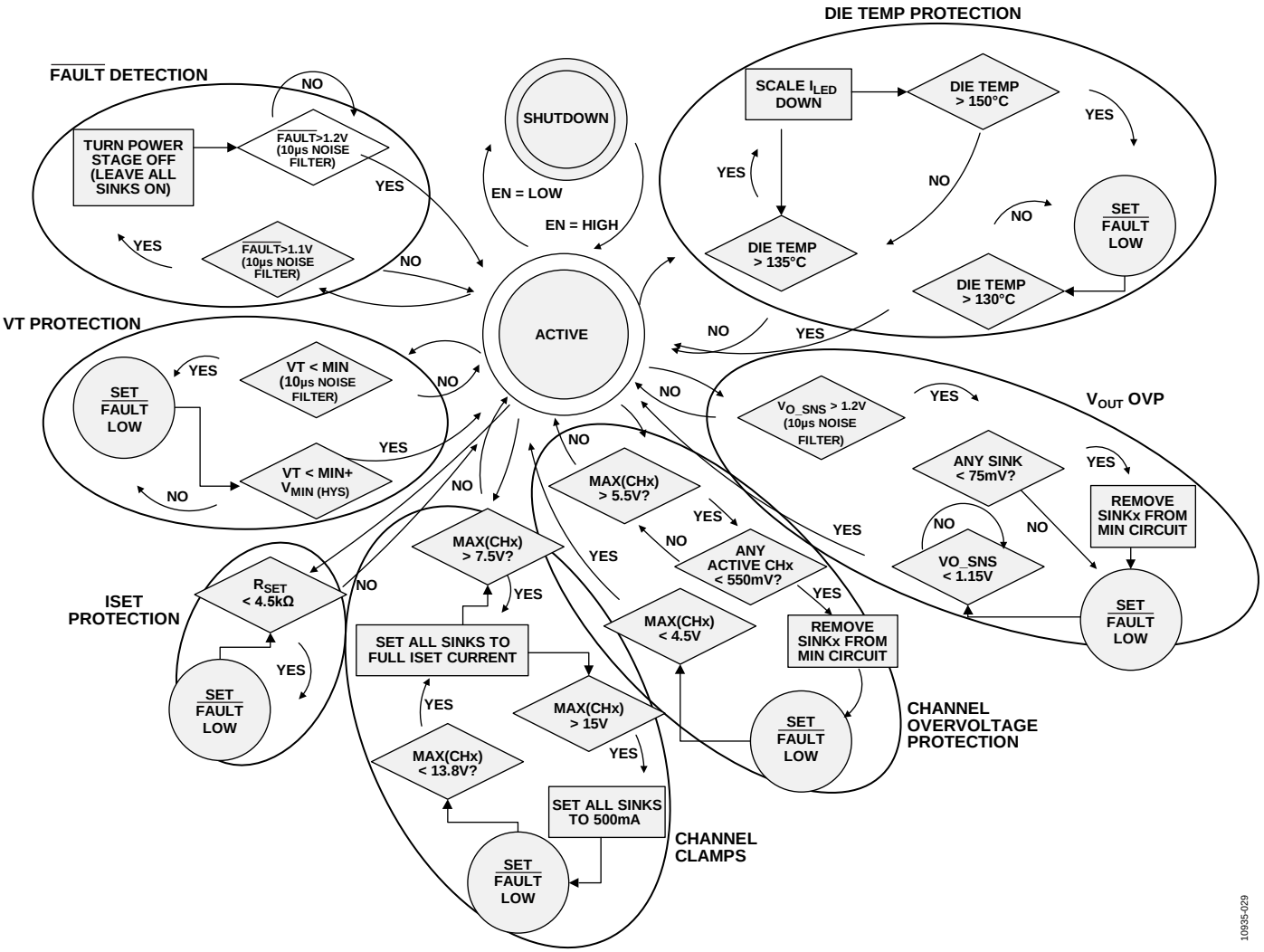

Figure 27. Fault Flowchart

LED OPEN-CIRCUIT AND SHORT-CIRCUIT PROTECTION

An LED open-circuit fault can result from a bad solder connection or damaged LED. An open LED string results in the current sink headroom falling to a very low level. The feedback loop naturally interprets this as a request for more power. This can quickly lead to a case where the output voltage is too high. However, on the ADP8140, any abnormally high output voltage is detected by the VO_SNS pin and the SINKx pins.

The VO_SNS pin senses the output voltage of the power supply through an external resistor divider. VO_SNS is then compared to an internal threshold (1.2 V typical). If the output voltage rises such that the voltage of the VO_SNS pin is greater than 1.2 V, an output overvoltage fault (VOUT_OVP) is declared. During a VOUT_OVP fault, any sinks with a voltage less than 80 mV (typical) are removed from the FB_OUT path. Then the FB_OUT pull-down NMOS is released and $\overline{\text{FAULT}}$ goes low, causing the power stage to shut down. The LED current sinks are left enabled during this event. When VO_SNS drops to 1.15 V (typical), the FB_OUT function resumes its normal operation and $\overline{\text{FAULT}}$ goes high.

Alternatively, the output voltage may not rise high enough to trigger the VO_SNS pin, but it may rise high enough to cause one of the SINKx pins to exceed 5.7 V (typical), or a shorted LED may cause the SINKx pins to exceed this level. To prevent excessive power dissipation and damage to the IC, when a SINKx pin rises above 5.7 V (typical), a channel overvoltage fault (CH_OVP) is declared. During a CH_OVP fault, any sinks with a voltage less than 525 mV (typical) are removed from the FB_OUT path. Then the FB_OUT pull-down NMOS is released, causing the power stage to shut down. The LED current sinks are left enabled during this event. When the SINKx voltage drops to 4.5 V (typical), the FB_OUT function resumes its normal operation.

Continued output overvoltage operation degrades efficiency and can affect the lifetime of passive components. Therefore, when an overvoltage condition is detected (either VOUT_OVP or CH_OVP), then any open LED current sinks are identified and removed from the feedback loop. But the sinks are always

left enabled, so that they can regulate the current if the open-circuit or short-circuit LED condition is removed. Bringing EN or VIN low and then high again restores all sinks to the feedback loop.

VO_SNS can also be used to monitor the input voltage. When connected to the input voltage through a resistor divider, the ADP8140 shuts down and disables any power stages if the supply input voltage rises too high. This shutdown can help to protect the LEDs and power stage.

DIE TEMPERATURE PROTECTION

Significant voltage mismatch between LED strings can create high power dissipation within the ADP8140. If this increase in power dissipation causes the die temperature on the ADP8140 to rise above 135°C (typical), the IC automatically begins to reduce the output current on all four sinks. If the die temperature continues to rise and exceeds 150°C (typical), the ADP8140 shuts down the power stage with COMP, FB_OUT, and $\overline{\text{FAULT}}$. When the temperature drops below 130°C (typical), the ADP8140 restarts the power stage. If the fault or high power dissipation persists, the sequence repeats.

USING MULTIPLE ADP8140 ICS

Multiple ADP8140 ICs can be combined in parallel to control the same supply. This combination is advantageous to control more than four strings of LEDs or to drive higher currents. For example, using two ADP8140 ICs, four LED strings can be driven at 1 A each, or two strings can be driven at 2 A each.

When using multiple ADP8140 ICs in parallel to control one power supply, all of the $\overline{\text{FAULT}}$ and EN pins must be connected together. If any $\overline{\text{FAULT}}$ pin goes low, all ADP8140 ICs respond to the event. Most applications will work best if the dimming signals are also connected amongst the ADP8140 ICs, though it is not required.

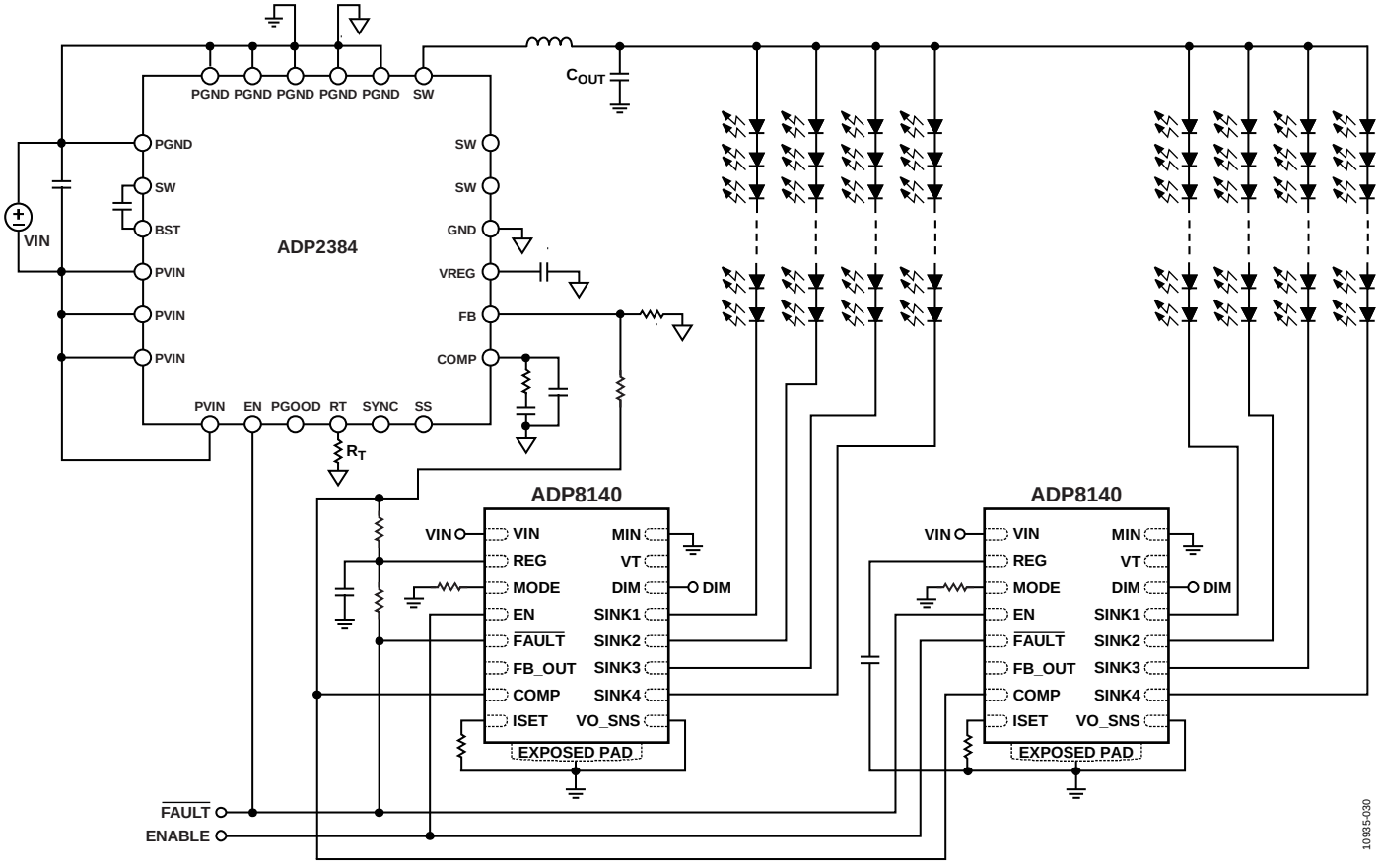

Figure 28. Multiple ADP8140 ICs Powered from One Supply (Low Gain Buffer Control Shown)

OPERATING THE ADP8140 FROM HIGHER INPUT VOLTAGES

The ADP8140 is capable of operating from an input voltage (V_{IN}) range of 3.0 V to 30 V. However, higher voltages can be used to power the ADP8140 when an appropriate current limiting circuit is used.

It is sometimes sufficient to limit the voltage on the VIN pin by placing a Zener diode on VIN and limiting the current with a resistor from the input voltage to the VIN pin. This method can be used if standby power dissipation is not an issue.

Alternatively, if the supply voltage range is small, an additional Zener diode between the supply and the VIN pin shifts the voltage at the VIN pin below 30 V. This method adds minimal power dissipation in both standby and active modes.

However, a more robust voltage limiter uses a Zener diode, an NPN transistor, and two resistors. This simple circuit, shown in Figure 29, gives the required operating I_Q during normal operation but also reduces the standby current when the ADP8140 is disabled.

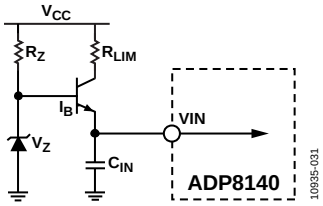

Figure 29. VIN Current Limiting Circuit for High Input Voltages

Select V_Z to give a voltage well below the 30 V absolute maximum of the VIN pin. With this circuit, the VIN pin voltage is regulated to about V_Z − 0.7 V. Select the resistor, R_Z, to limit the current when the ADP8140 is disabled yet still provide enough current to reverse bias the Zener diode and drive the NPN transistor when the ADP8140 is active. The current through R_Z is given by

$$I_{RZ} = \left(\frac{V_{CC} - V_Z}{R_Z} \right)$$

A value of 100 µA at the minimum expected V_{CC} is generally sufficient. Even at maximum V_{CC}, this value only contributes a few milliwatts of power dissipation during standby.

R_{LIM} limits the maximum current during transients. A value of a few hundred ohms is sufficient. When the ADP8140 is active, the additional worst case power dissipation from this limit circuitry is given by

$$\Delta P_{DISS(ACTIVE)} = (V_{CC(MAX)} - V_{Z(MIN)} + 0.7\ \text{V}) \times I_Q = (48\ \text{V} - 24\ \text{V} + 0.7\ \text{V}) \times 3\ \text{mA} = 74\ \text{mW}$$

EFFECT OF LED V_F MISMATCH

The ADP8140 always controls the FB_OUT pin to regulate the output voltage to provide the minimum amount of headroom voltage required for the current sinks. One of the current sinks is regulated to $V_{EA(REF)}$. Typically, $V_{EA(REF)}$ is either 350 mV or 450 mV (see $V_{EA(350)}$ and $V_{EA(450)}$ in Table 1). The voltage seen on the other three SINKx pins varies based on the distribution of the LED forward voltage, V_F. For a given lot of LEDs, the V_F and the change in V_F with temperature is relatively consistent. Given a V_F distribution, the maximum voltage that appears on any of the SINKx pins can be statistically calculated. For example, consider a mean V_F of 3.5 V and a normal distribution with a standard deviation of 70 mV. A statistical analysis of such a distribution reveals the maximum voltage that may appear on any of the SINKx pins, as shown in Figure 30). Note that in Figure 30, the maximum value is defined as the average plus six standard deviations (σ) of the distribution.

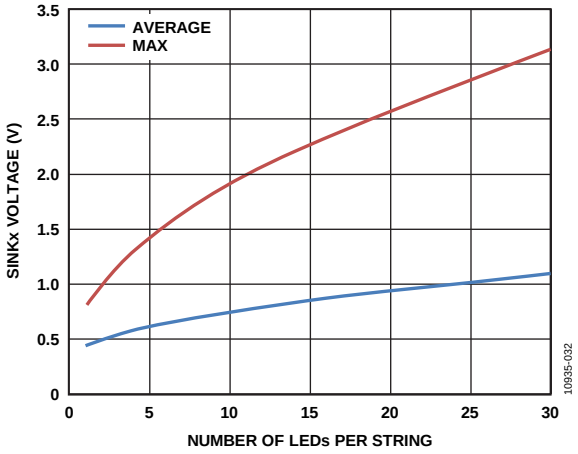

Figure 30. Voltage on SINKx Pins Given a Normal Distribution of V_F, Standard Deviation = 70 mV

The SINKx voltage found on each pin determines the power that the ADP8140 package must dissipate. Specifically, the ADP8140 power dissipation can be represented as follows:

$$P_{DISS} = (V_{SINK1} + V_{SINK2} + V_{SINK3} + V_{SINK4}) \times I_{LED} \quad (2)$$

A statistical analysis based on the V_F distribution of the LED can be performed to predict the total power dissipation within the ADP8140. For the same distribution used in Equation 2 and an LED current of 350 mA, Figure 31 gives the average and maximum power dissipations. Note that in Figure 31, the maximum value is defined as the average plus six standard deviations of the distribution.

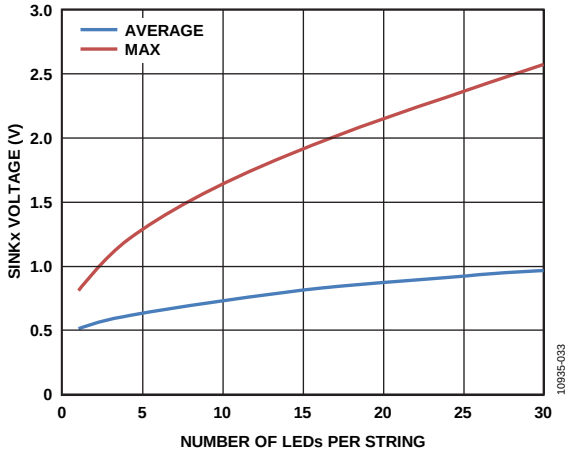

Figure 31. Total Power Dissipation (All Four Strings) for a Normal Distribution of V_F, Standard Deviation = 70 mV, I_{LED} = 350 mA

MANAGING THE POWER DISSIPATION OF THE ADP8140

With the predicted power dissipation known, the next step is to determine if the ADP8140 package is able to dissipate that power adequately. Use the following to calculate the maximum power that the ADP8140 is able to dissipate:

$$P_{DISS(MAX)} = (T_J - T_{BOARD})/\theta_{JB}$$
$$= (135 - 105)/12.4 = 2.4 \text{ W}$$

where:
T_J =135°C, the maximum ADP8140 junction temperature (before entering thermal foldback).
T_{BOARD} = 105°C, the maximum board temperature.
θ_{JB} = 12.4°C/W (see Table 3).

Assume that 100% of the power dissipates through the exposed pad to the board.

The ability of the ADP8140 package to dissipate heat varies if the operating conditions are not consistent with the θ_{JB} conditions given in Table 3. Additionally, it is imperative to follow the layout guidelines given in the Layout Guidelines section.

LAYOUT GUIDELINES

For optimum performance, follow these layout guidelines:

- The exposed pad of the ADP8140 must be properly connected to a heat sink. Solder the exposed pad to the PCB and connect it to a large plane of ground metal with an array of thermal vias.
- The ADP8140 is designed for easy layout with single sided metal core substrates. If FR4 substrate is used, thermal vias must be used between the LFCSP exposed pad and a large ground trace on the opposite side of the board.
- Place the REG capacitor close to the IC. The location of the VIN capacitor is not as important.
- Place the COMP capacitor(s) and resistor as close to the IC as possible.
- Place the VO_SNS resistors (if used) close to the IC.
- If applying an analog dimming voltage to the DIM or VT pins, placing a bypass capacitor near these pins reduces the noise on these dimming signals.

ORDERING OPTIONS

The ADP8140 is available in two options. The difference between the options is the $V_{EA(REF)}$ voltage and the number of sinks that control the COMP and FB_OUT voltage.

See Figure 33 to Figure 36 for examples of the ADP8140 used in various configurations: with a PMOS regulation stage, as a secondary side controller, with a boost or buck power stage, or with one power stage.

ADP8140ACPZ-1-R7

The ADP8140ACPZ-1-R7 has $V_{EA(REF)}$ at 350 mV. Therefore, if using the device with the PMOS power stage or as a secondary side controller, each current sink can supply up to 350 mA of LED current at 350 mV of headroom voltage. However, if using the device to control an SMPS IC, each current sink can supply up to 500 mA of LED current.

The minimum voltage for all four of the current sinks is used to control the power regulation (COMP and FB_OUT).

ADP8140ACPZ-2-R7

The ADP8140ACPZ-2-R7 has $V_{EA(REF)}$ at 450 mV. Therefore, all four of the sinks can be driven to 500 mA in any configuration.

Only the minimum voltage from SINK1, SINK2, and SINK3 is used to control the FB_OUT and COMP pins. Therefore, this is the preferred device model if only three LED strings are used in a system. SINK4 can be left floating or connected to GND. Note that SINK4 is still enabled; if it is connected to an LED string, it regulates its current to be the same as the other sinks. Therefore, SINK4 can be combined with another SINKx pin (for example to drive two strings at 1 A each).

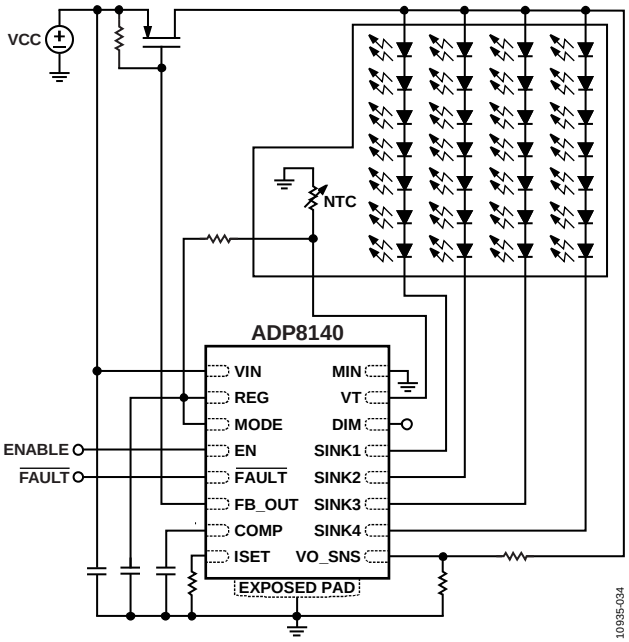

Figure 32. ADP8140 with a PMOS Regulation Stage

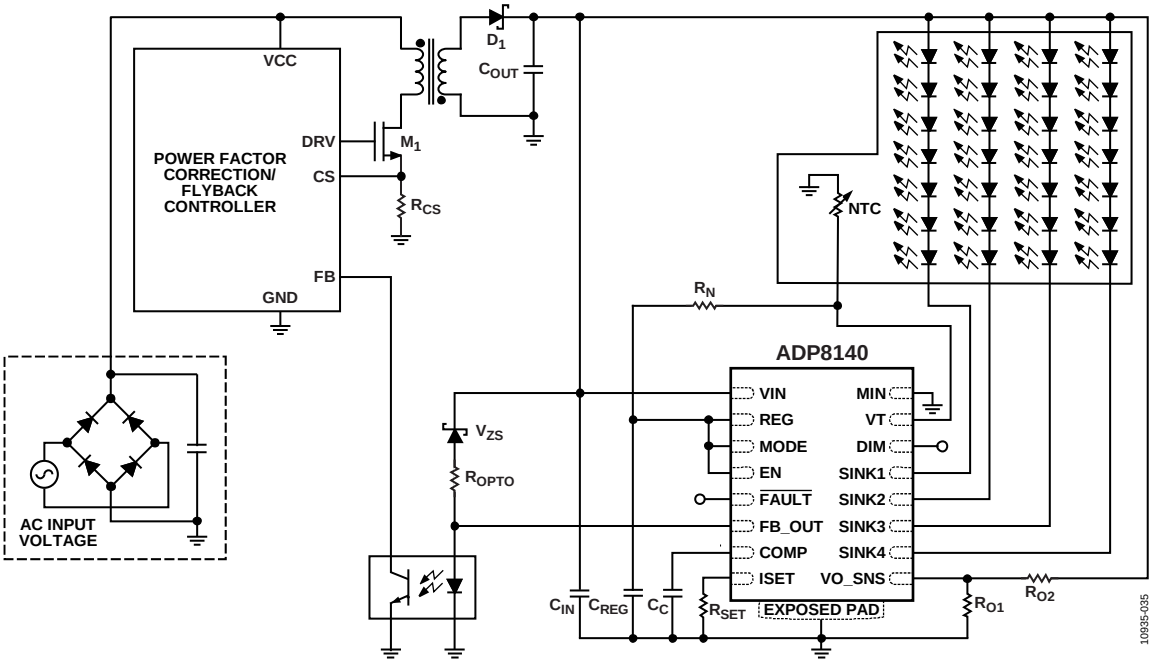

Figure 33. ADP8140 Secondary Side Control Design Example

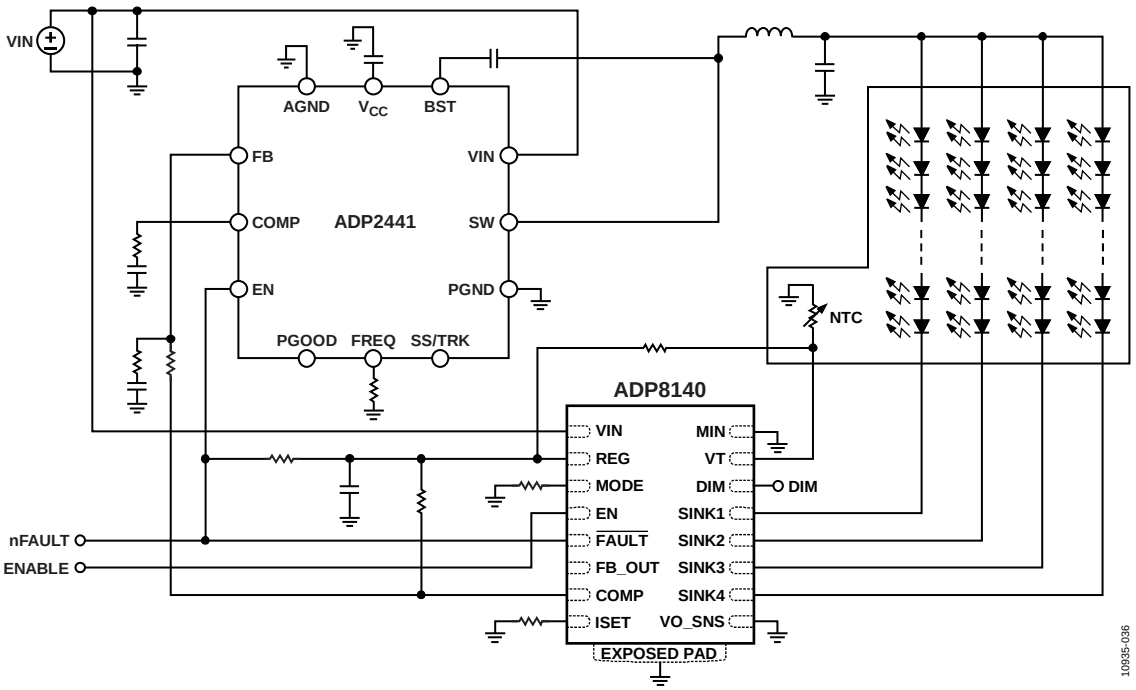

Figure 34. ADP8140 with a Buck Power Stage

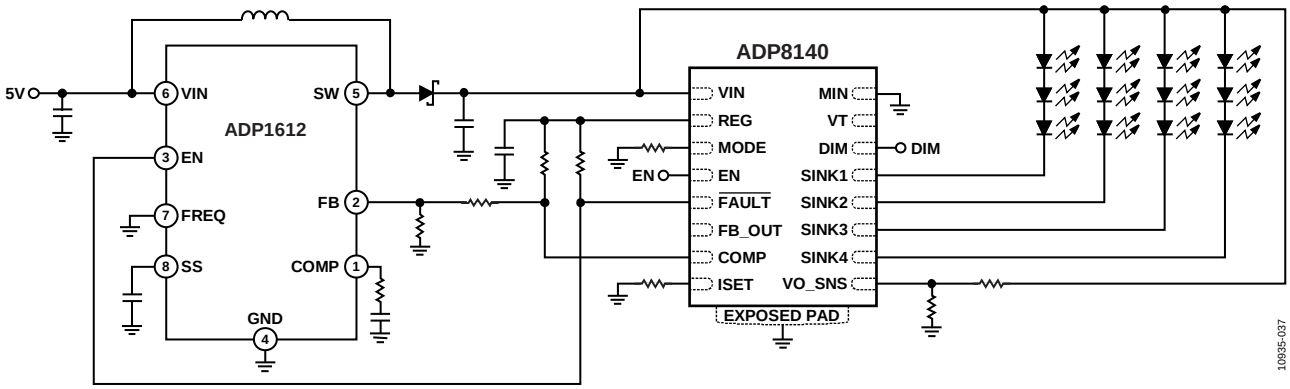

Figure 35. ADP8140 with a Boost Power Stage

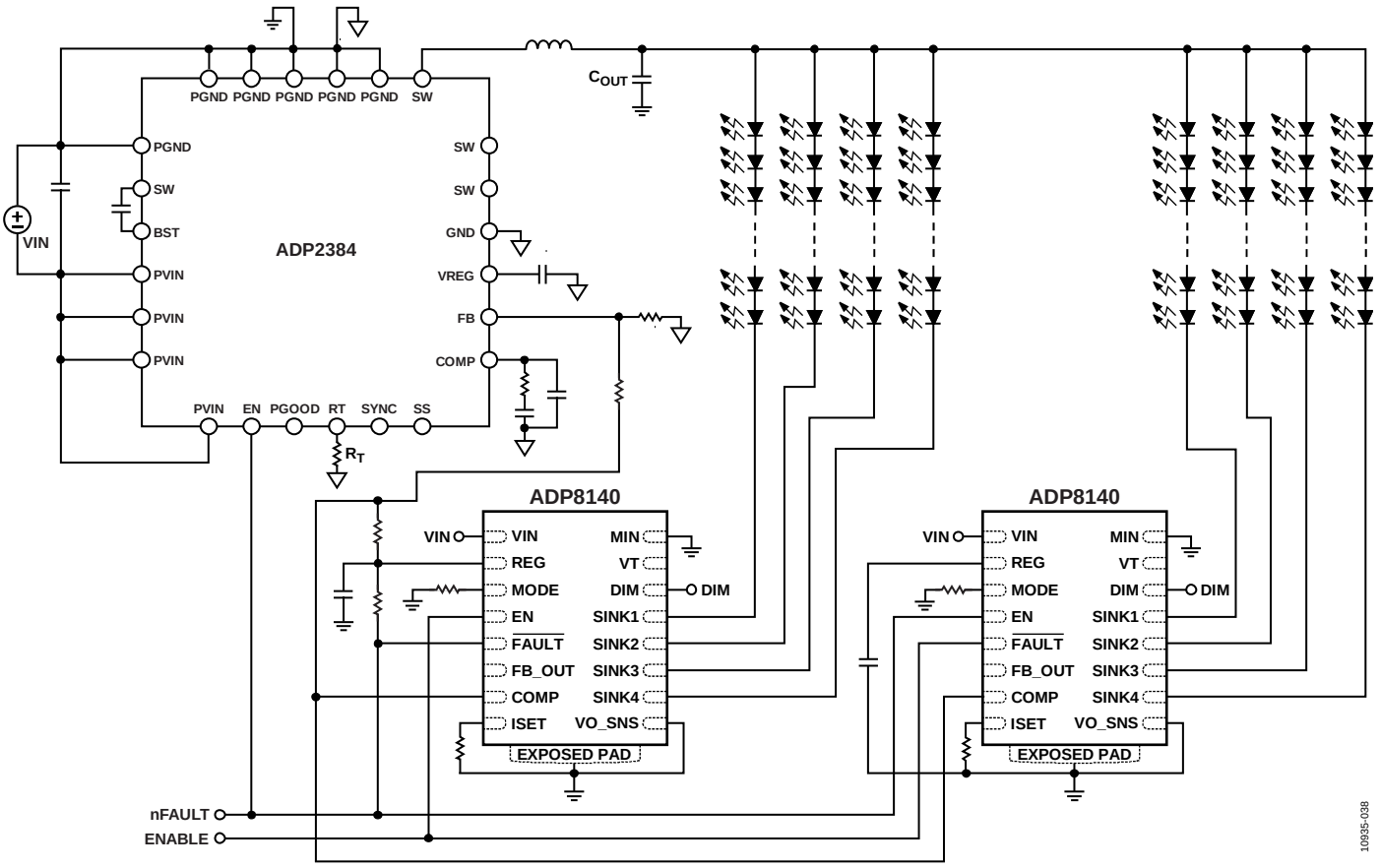

Figure 36. Multiple ADP8140 ICs with One Power Stage

OUTLINE DIMENSIONS

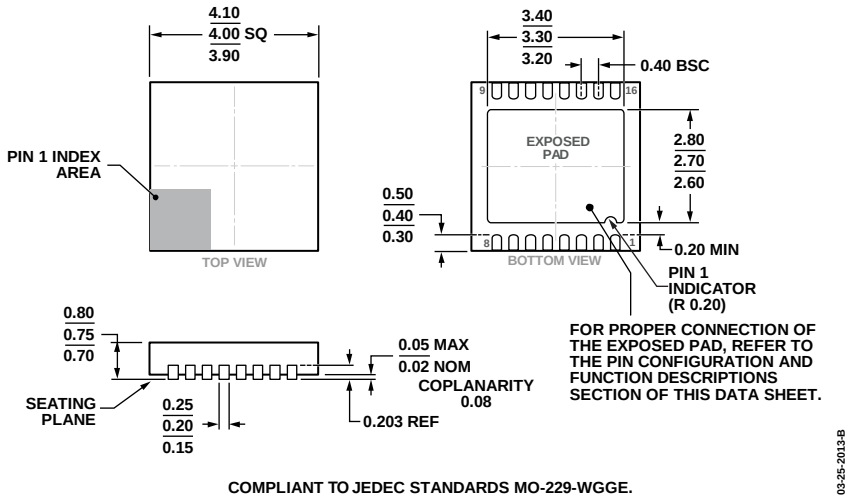

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP_WD]
4 mm × 4 mm Body, Very Very Thin Dual
(CP-16-29)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	$V_{EA(REF)}$ (mV)	Temperature Range	Package Description	Package Option
ADP8140ACPZ-1-R7	350	−40°C to +125°C	16-Lead LFCSP_WD, 7″ Tape and Reel	CP-16-29
ADP8140ACPZ-2-R7	450	−40°C to +125°C	16-Lead LFCSP_WD, 7″ Tape and Reel	CP-16-29
ADP8140EB-EVALZ			ADP8140 PMOS Evaluation Board	
ADP8140CP-EVALZ			ADP8140EB-EVALZ with the LEDs and Heat Sink	
ADP8140EB2-EVALZ			ADP8140 Buck Evaluation Board	
ADP8140CP2-EVALZ			ADP8140EB2-EVALZ with the LEDs and Heat Sink	

[1] Z = RoHS Compliant Part.
[2] ADP8140ACPZ-1-R7: SINK4 function is normal.
[3] ADP8140ACPZ-2-R7: SINK4 regulates current but does not control FB_OUT and COMP.