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Kind regards,

Team Nexperia

# PHP18NQ11T

## N-channel TrenchMOS standard level FET

Rev. 02 — 10 March 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- Class-D audio amplifiers
- DC-to-DC convertors
- Inverters
- Switched-mode power supplies

### 1.4 Quick reference data

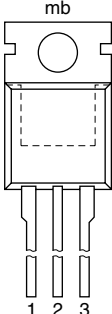
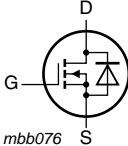
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	110	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	18	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	79	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 18\text{ A}$ ; $V_{DS} = 80\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	8	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 9\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	80	90	m $\Omega$



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT78 (TO-220AB)**

## 3. Ordering information

Table 3. Ordering information

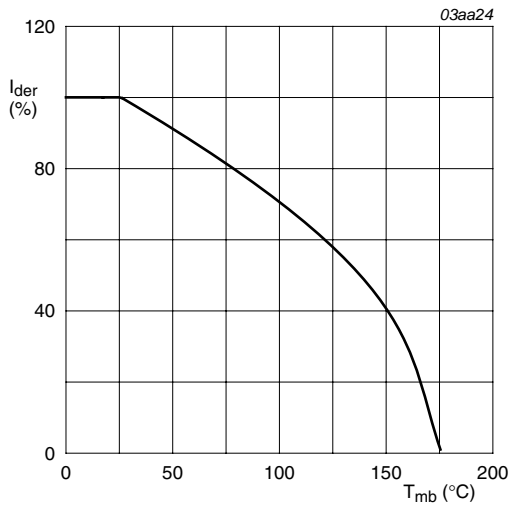
Type number	Package		
	Name	Description	Version
PHP18NQ11T	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

## 4. Limiting values

Table 4. Limiting values

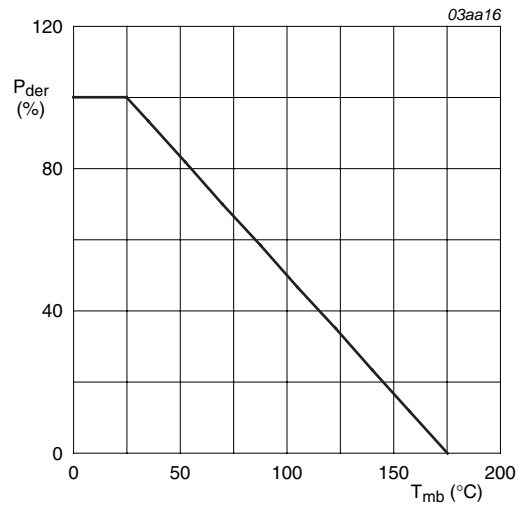
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	110	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	110	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	13	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	18	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	72	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	79	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	18	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	72	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 11\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.1\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	70	mJ



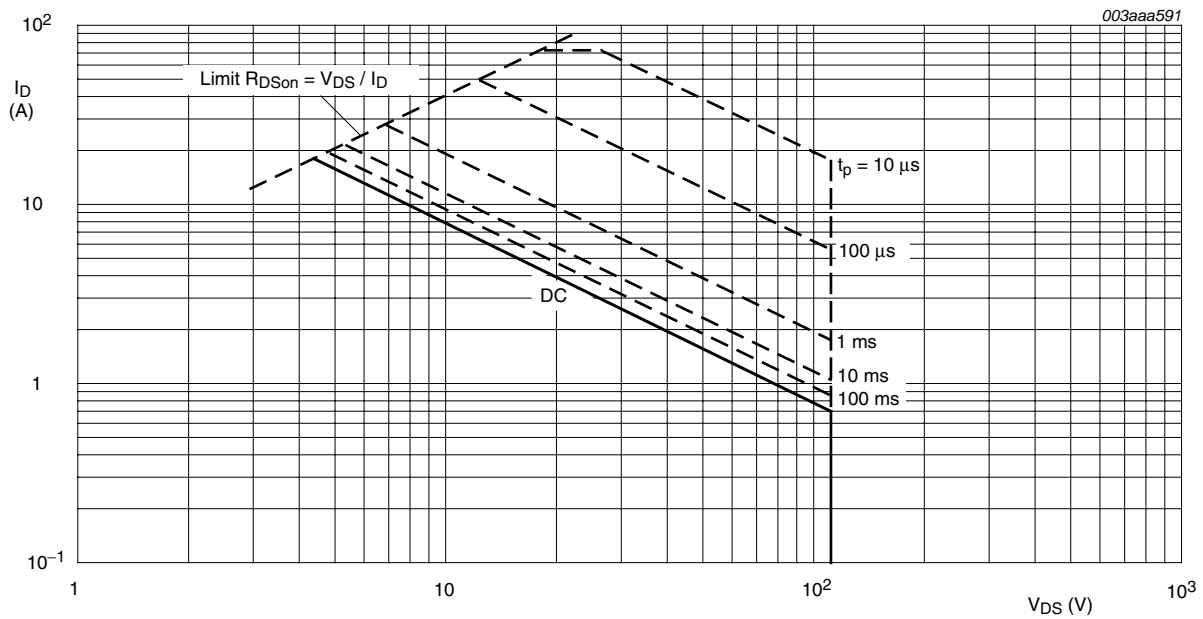
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ C; I_{DM}$  is single pulse;  $V_{GS} = 10V$

Fig 3. Safe operating area: continuous and peak currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

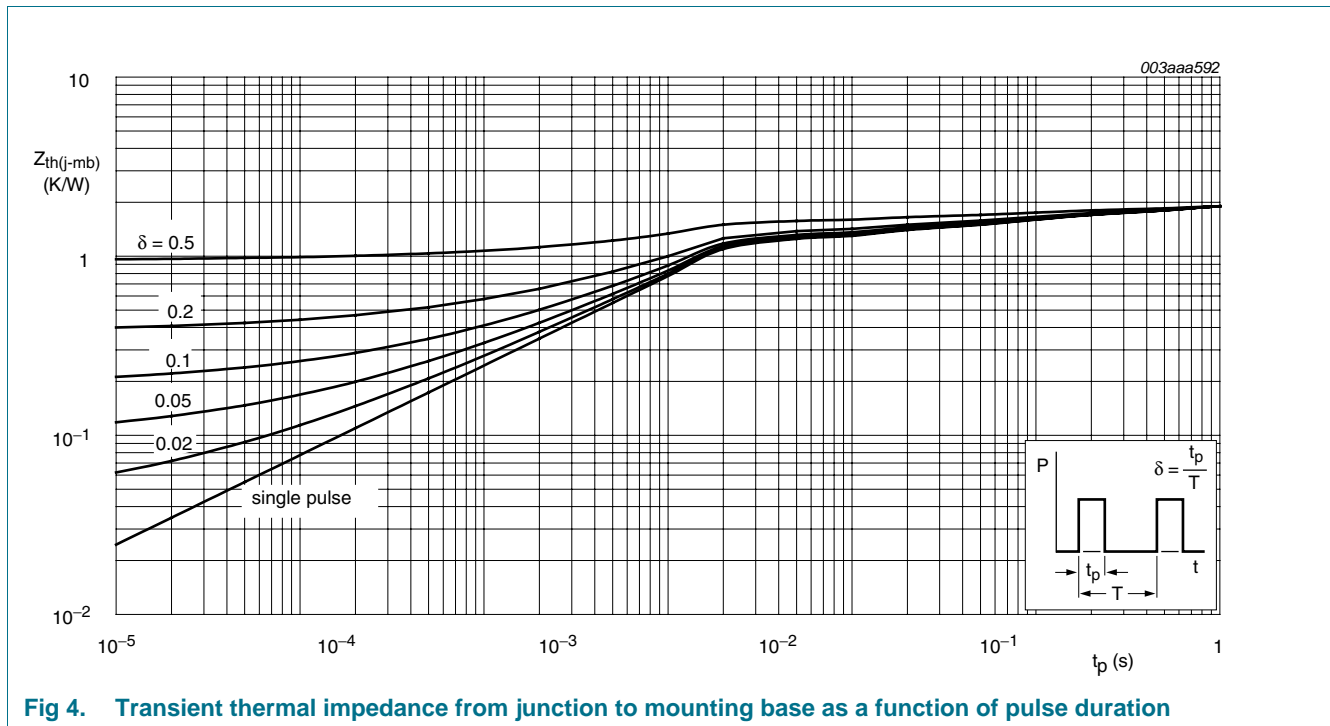
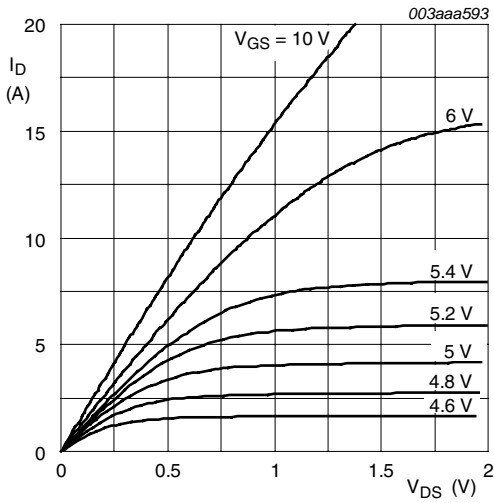


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

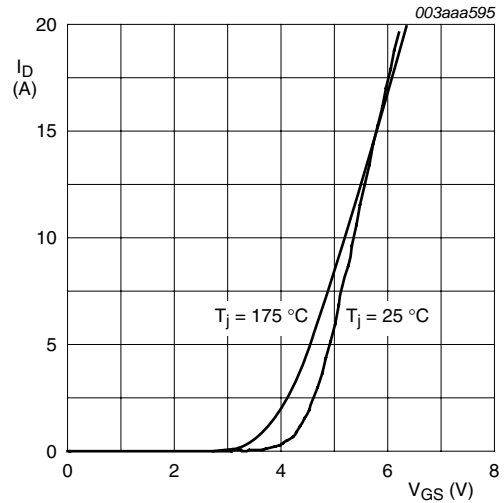
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	98	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 110 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.05	10	$\mu A$
		$V_{DS} = 110 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 9 A; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	-	243	m $\Omega$
		$V_{GS} = 10 V; I_D = 9 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	80	90	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 18 A; V_{DS} = 80 V; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	21	-	nC
$Q_{GS}$	gate-source charge		-	4	-	nC
$Q_{GD}$	gate-drain charge		-	8	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	633	-	pF
$C_{oss}$	output capacitance		-	103	-	pF
$C_{rss}$	reverse transfer capacitance		-	61	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 V; R_L = 2.7 \text{ } \Omega; V_{GS} = 10 V; R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ C; I_D = 18.5 A$	-	6	-	ns
$t_r$	rise time		-	36	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 18 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	0.92	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 18 A; di_S/dt = 100 A/\mu s; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 \text{ }^\circ C$	-	55	-	ns
$Q_r$	recovered charge		-	135	-	nC



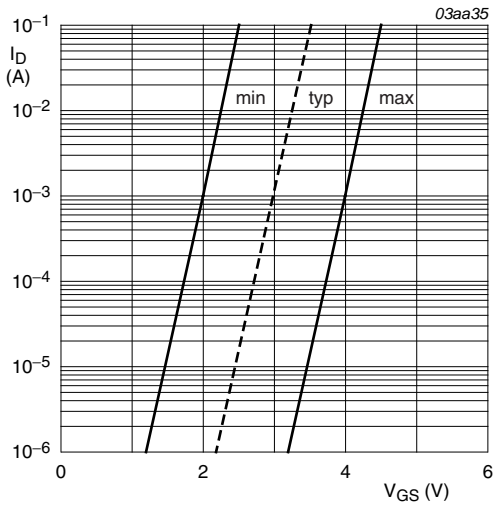
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



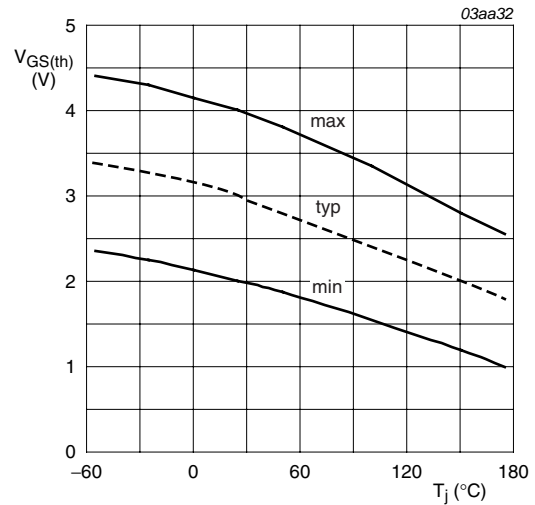
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



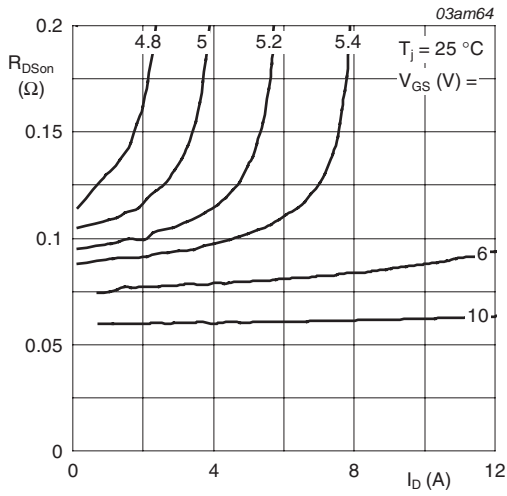
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



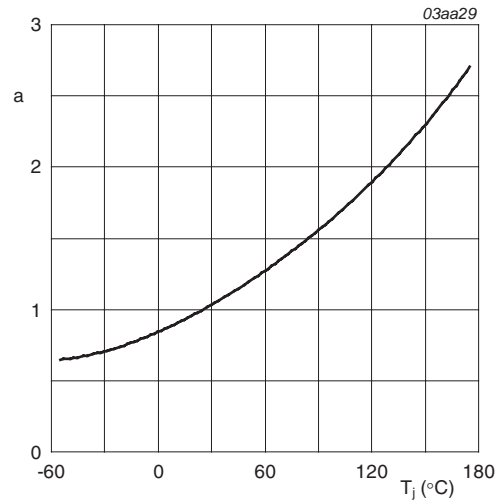
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



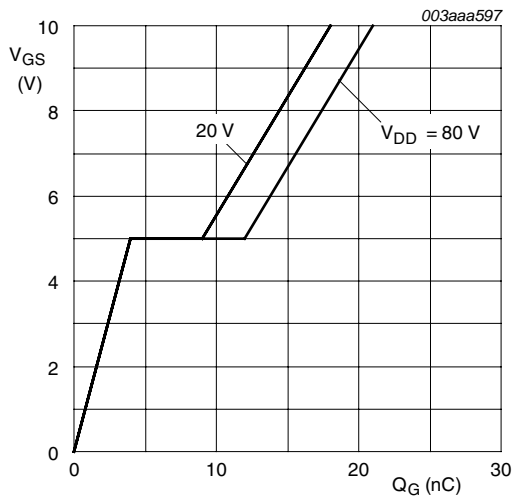
$T_j = 25^\circ\text{C}$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



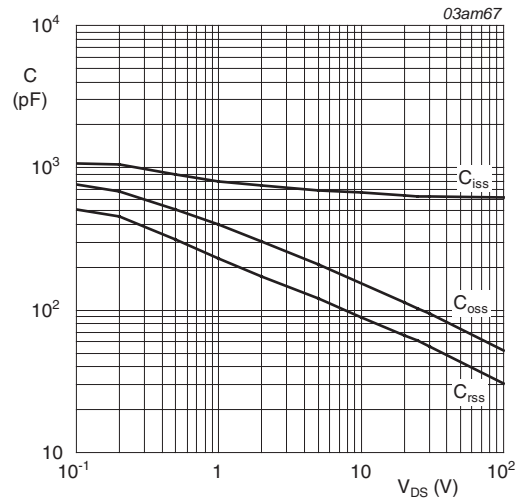
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



$I_D = 3\text{A}; V_{DD} = 20\text{V and } 80\text{V}$

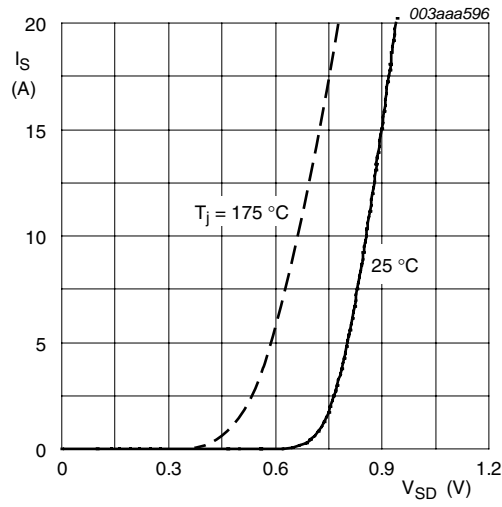
**Fig 11. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





$T_j = 25^{\circ}\text{C}$  and  $175^{\circ}\text{C}; V_{GS} = 0\text{V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

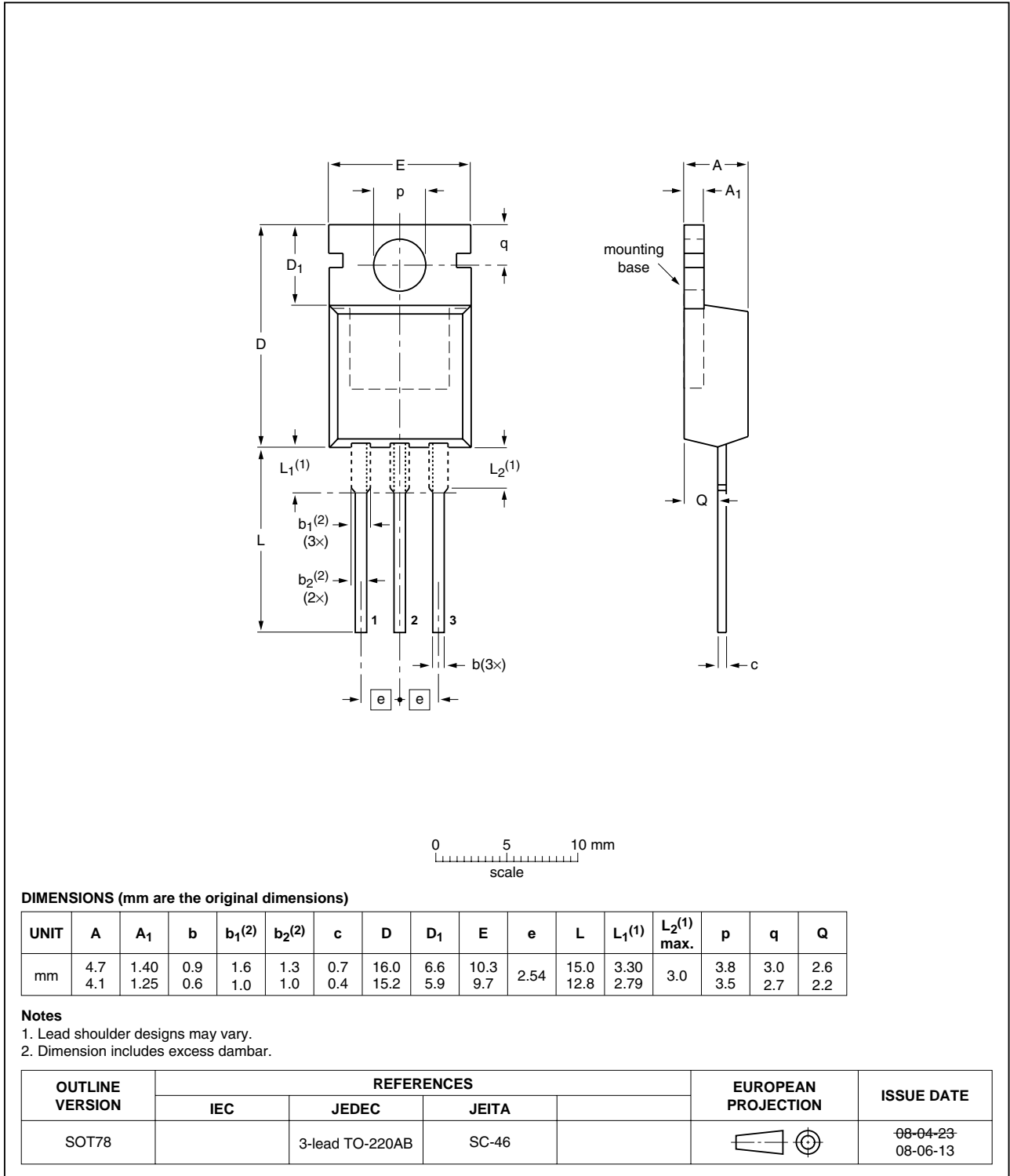


Fig 14. Package outline SOT78 (TO-220AB)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHP18NQ11T_2	20100310	Product data sheet	-	PHP18NQ11T-01
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>
PHP18NQ11T-01 (9397 750 12305)	20031113	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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