MC33978ER

MC33978 mask N11P errata

Rev. 2.0 — 11 January 2017 Errata sheet

Document information

Information	Content
Keywords	MC33978EK, MC34978EK, PC33978ES, MC33978AEK, MC33978AES, MC34978AEK, MC34978AES
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

1 Revision history

Table 1. Revision history

Rev	Date	Description
1.0	6/2015	• Initial release
	8/2016	• Updated to NXP document form and style
2.0	1/2017	• Updated document format • Added ER02 as per CIN # 201612010I

2 Product identification

This errata document applies to the following SMARTMOS devices:

Table 2. Orderable part number identification

Part number	Version	Mask ID	Package	Chip marking
MC33978EK	P2.1	N11P	32-pin SOICW-EP	MC33978EK
MC34978EK	P2.1	N11P	32-pin SOICW-EP	MC34978EK
PC33978ES[1]	P2.1	N11P	32-pin QFN (WF-type)	PC33978
MC33978AEK	P2.2	N11P	32-pin SOICW-EP	MC33978AEK
MC33978AES	P2.2	N11P	32-pin QFN (WF-TYPE)	M33978A
MC34978AEK	P2.2	N11P	32-pin SOICW-EP	MC34978AEK
MC34978AES	P2.2	N11P	32-pin QFN (WF-TYPE)	M34978A

[1] For the QFN version (suffix ES), ER01 applies to pre-production (PC) samples only.

2.1 Device part number prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices are marked with the MC prefix.

2.2 Device build information / date code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1025”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1025” indicates the 25th week of the year 2010.

3 Errata overview

Table 3. Functional problems table

Functional problems	Short description	Severity level [1][2][3][4]	Solution	Detailed description
ER01	WAKE_B fails to pull-down in normal mode without V_{DDQ}	Medium	Fix in silicon revision P2.2	Section 4.1
ER02	AMUX output voltage deviates when there are negative inputs on SGx or SPx	Low	None	Section 4.2

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device
[4] Enhancement: Improvement made to the device due to previously found issues on the design

4 Functional problems description

4.1 ER01—WAKE_B fails to pull-down in normal mode without V_{DDQ}

4.1.1 Severity level

Medium

4.1.2 Introduction

When operating as an OUTPUT, WAKE_B may exhibit erratic behavior under the following circumstances:

- The MC33978 is in LPM, WAKE_B is released and is expected to be pulled up externally to V_{BATP} to assert the ENABLE_B of the external V_{DDQ} regulator HIGH, which turns the V_{DDQ} rail OFF.
- A switch change is detected. The device wakes up from LPM but WAKE_B is unable to be pulled down to 0 V and fails to enable the V_{DDQ} regulator. Hence no complete system wake-up is possible.

4.1.3 Problem

The WAKE_B internal block is currently powered by V_{DDQ}. When V_{DDQ} is lost, there is no signal to drive the gate of the open drain FET and pull the WAKE_B pin low.

This issue is present solely at the system level and only impacts applications implementing the WAKE_B as the control signal for the V_{DDQ} voltage rail. For those applications in which V_{DDQ} is always ON, this issue should not be a problem.

4.1.4 Work-around

No work-around

4.1.5 Fix plan

Will be fixed in silicon 2.2

4.2 ER02—AMUX output voltage deviates when there are negative inputs on SGx or SPx

4.2.1 Severity level

Low

4.2.2 Introduction

AMUX output voltage deviates when there are negative inputs on other SGx or SPx channels.

By design, the multiplexer for AMUX operates only in the positive 0 V to 5.0 V range and does not take into account negative inputs. From that perspective, it works as designed. However, in customer applications that exclude the AMUX channel, the other SGx and SPx pins are allowed a minimum –1.0 V negative input. The SGx or SPx negative inputs may cause the AMUX output to deviate from its input.

4.2.3 Problem

Negative voltages are turning on parasitic devices on SGx/SPx channels, causing AMUX input voltage error.

This issue is present at the system level and only impacts applications in which the MCU reads the AMUX when there is negative input on other SGx or SPx channels. This issue is not a problem for those applications in which AMUX is not used or negative inputs are not present on SGx or SPx.

4.2.4 Work-around

The MCU should read the AMUX only when no negative offset is present on any of the SGx/SPx input pins

4.2.5 Fix plan

None

5 Legal information

5.1 Definitions

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