PIC18F1230/1330

PIC18F1230/1330 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39758**C**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F1230/1330 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Oscillator Configurations – PLL

The second paragraph of **Section 2.6.4 "PLL in INTOSC Modes"**, is modified by the addition of new text shown in bold.

Unlike HSPLL mode, the PLL is controlled through software. The control bit, PLLEN (OSCTUNE<6>), is used to enable or disable its operation. **If PLL is enabled and a Two-Speed Start-up from wake is performed, execution is delayed until the PLL starts.**

2. Module: Flash Program Memory

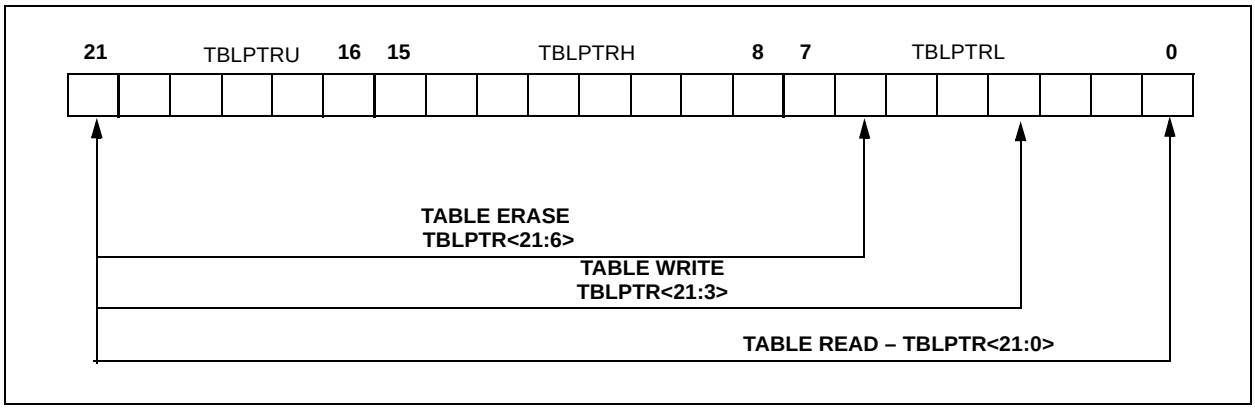
In **Section 6.2.4 "Table Pointer Boundaries"**, the third paragraph and Figure 6-3 are modified:

- The paragraph is modified by the removal of the first sentence and the addition of new text shown in bold.

When the timed write to program memory begins (via the WR bit), the 19 MSbs of the TBLPTR (TBLPTR<21:3>) determine which program memory block of 8 bytes is written to. **The Table Pointer register's three LSBs (TBLPTR<2:0>) are ignored.** For more detail, see **Section 6.5 "Writing to Flash Program Memory"**.

- Figure 6-3 is modified as shown.

FIGURE 6-3: TABLE POINTER BOUNDARIES BASED ON OPERATION



3. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

The BAUDCON register is changed to add one bit and rename another:

- Added bit – Bit 5, previously unimplemented, is now RXDTP
- Renamed bit – Bit 4, previously SCKP, is now TXCKP

The TXCKP and RXDTP bits allow the Asynchronous mode TX and RX signals to be inverted (polarity reversed). RXDTP has no effect on the Synchronous mode DT signal.

The register table and new bit descriptions appear as shown.

REGISTER 14-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 5 **RXDTP:** Received Data Polarity Select bit

Asynchronous mode:
1 = RX data is inverted
0 = RX data is *not* inverted

Synchronous mode:
Unused in this mode

bit 4 **TXCKP:** Clock and Data Polarity Select bit

Asynchronous mode:
1 = TX data is inverted
0 = TX data is *not* inverted

Synchronous mode:
1 = CK clocks are inverted
0 = CK clocks are *not* inverted

4. Module: 10-Bit Analog-to-Digital Converter (A/D)

Register 15-2 is modified as shown to:

- Change the bit designations of ADCON<2:0> (PCFG2, PCFG1 and PCFG0) to R/W-0, to match PCFG3 (ADCON<3>)
- Remove the notes for ADCON<3:0>

The new text appears in bold.

REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-**0**	R/W-**0**	R/W-**0**
—	—	—	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = Positive reference for the A/D is V_{REF+}
0 = Positive reference for the A/D is AV_{DD}

bit 3 **PCFG3:** A/D Port Configuration bit for RA6/AN3
0 = Port is configured as AN3
1 = Port is configured as RA6

bit 2 **PCFG2:** A/D Port Configuration bit for RA4/AN2
0 = Port is configured as AN2
1 = Port is configured as RA4

bit 1 **PCFG1:** A/D Port Configuration bit for RA1/AN1
0 = Port is configured as AN1
1 = Port is configured as RA1

bit 0 **PCFG0:** A/D Port Configuration bit for RA0/AN0
0 = Port is configured as AN0
1 = Port is configured as RA0

5. Module: Comparator

In **Section 16.6 "Comparator Interrupts"**, the procedure for clearing the interrupt in the Interrupt Service Routine is modified with the new text shown in bold.

a) End the mismatch condition by doing either of the following:
   - Reading or writing to CMCON
   - **Returning the input to its original state**

b) Clear flag bit CMPxIF

6. Module: Comparator Voltage Reference

Section 17.1 "Configuring the Comparator Voltage Reference" is changed to:

- Add new text and a table (Table 17-1) about the voltage reference being able to select the unscaled V_{REF+} for comparator input
- Modify Register 17-1 (CVRCON) with a new description of bit 4 (CVRSS)
- Revise Figure 17-1

The textual changes break the last sentence of the first paragraph of **Section 17.1 "Configuring the Comparator Voltage Reference"** into a second paragraph and adds content. The incorporation of the three bulleted changes are shown, with new or altered text indicated by bold face.

The equations used to calculate the output of the comparator voltage reference are as follows:

If CVRR = 1:
$CV_{REF} = ((CVR3:CVR0)/24) \times CV_{RSRC}$
If CVRR = 0:
$CV_{REF} = (CV_{RSRC} \times 1/4) + (((CVR3:CVR0)/32) \times CV_{RSRC})$

The comparator reference supply voltage can come from either AV_{DD} or AV_{SS}, or the external $V_{REF}+$ that is multiplexed with RA4 and AV_{SS}. The voltage source is selected by the CVRSS bit (CVRCON<4>).

Additionally, the voltage reference can select the unscaled $V_{REF}+$ input for use by the comparators, bypassing the CV_{REF} module. (See Table 17-1 and Figure 17-1.)

TABLE 17-1: VOLTAGE REFERENCE OUTPUT

CVREN	CVRSS	CV_{REF}	Comparator Input
0	0	Disabled	No reference
0	1	Disabled	From V_{REF} (CV_{REF} bypassed)
1	0	Enabled	From CV_{REF}
1	1	Enabled	From CV_{REF}

REGISTER 17-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	—	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CVREN**: Comparator Voltage Reference Enable bit
1 = CV_{REF} circuit powered on
0 = CV_{REF} circuit powered down

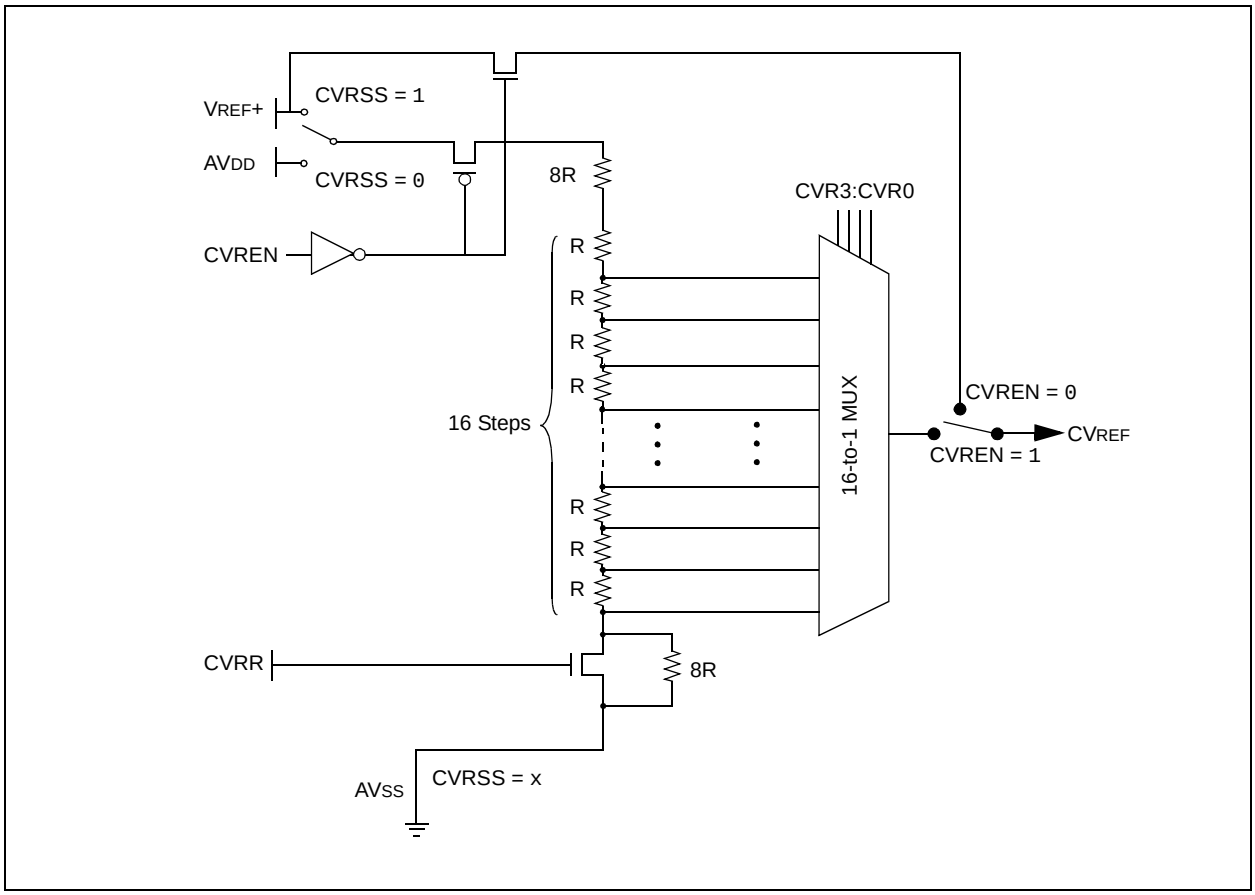
bit 6 **Unimplemented:** Read as '0'

bit 5 **CVRR**: Comparator V_{REF} Range Selection bit
1 = 0 to 0.667 CV_{RSRC}, with CV_{RSRC}/24 step size (low range)
0 = 0.25 CV_{RSRC} to 0.75 CV_{RSRC}, with CV_{RSRC}/32 step size (high range)

bit 4 **CVRSS**: Comparator V_{REF} Source Selection bit
When CVRR = 1:
1 = Comparator reference source, $CV_{RSRC} = (V_{REF}+) - (AV_{SS})$
0 = Comparator reference source, $CV_{RSRC} = AV_{DD} - AV_{SS}$
When CVRR = 0:
1 = $V_{REF}+$ input used directly, comparator voltage reference bypassed
0 = No reference is provided

bit 3-0 **CVR3:CVR0:** Comparator V_{REF} Value Selection bits ($0 \le (CVR3:CVR0) \le 15$)
When CVRR = 1:
$CV_{REF} = ((CVR3:CVR0)/24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = (CV_{RSRC}/4) + ((CVR3:CVR0)/32) \bullet (CV_{RSRC})$

FIGURE 17-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



7. Module: Special Features of the CPU

The bit descriptions for Register 19-6, Register 19-13 and Register 19-14 are changed as indicated by the bold and bold and underlined text.

REGISTER 19-6: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	R/P-0	R/P-0	R/P-0	U-0	U-0	U-0	R/P-1
$\overline{\text{BKBUG}}$	XINST	BBSIZ1	BBSIZ0	—	—	—	STVREN
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7 **$\overline{\text{BKBUG}}$:** Background Debugger Enable bit
1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins
0 = Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug

bit 6 **XINST:** Extended Instruction Set Enable bit
1 = Instruction set extension and Indexed Addressing mode enabled
0 = Instruction set extension and Indexed Addressing mode disabled

bit 5-4 **BBSIZ<1:0>:** Boot Block Size Select bits
For PIC18F1330 device:
11 = 1 kW Boot Block size
10 = 1 kW Boot Block size
01 = 512W Boot Block size
00 = 256W Boot Block size
For PIC18F1230 device:
11 = 512W Boot Block size
10 = 512W Boot Block size
01 = 512W Boot Block size
00 = 256W Boot Block size

bit 3 Unimplemented: Maintain as ‘0’

bit 2-1 Unimplemented: Read as ‘0’

bit 0 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Reset on stack overflow/underflow enabled
0 = Reset on stack overflow/underflow disabled

REGISTER 19-13: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F1230/1330 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-5 **DEV2:DEV0:** Device ID bits
000 =PIC18F1230
001 =PIC18F1330

bit 4-0 **REV4:REV0:** Revision ID bits
These bits are used to indicate the device revision.

REGISTER 19-14: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F1230/1330 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits(1)
0001 1110 = PIC18F1230/1330 devices
These bits are used with the DEV2:DEV0 bits in the DEVID1 register to identify part number.

Note 1: The values for DEV10:DEV3 may be shared with other devices. A device can be identified by using the entire, DEV10:DEV0 bit sequence.

8. Module: Electrical Characteristics

In Table 22-1, the values for the D122 and D133A parameters are changed as indicated by bold text.

TABLE 22-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C to +85°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	**3.59**	**4.10**	**4.86**	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C to +85°C
D125	IDDP	Supply Current during Programming	—	10	—	mA	
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132B	VPEW	VDD for Self-Timed Write	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D133A	TIW	Self-Timed Write Cycle Time	**1.79**	**2.05**	**2.43**	ms	
D134	TRETD	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Refer to Section 7.8 for a more detailed discussion on data EEPROM endurance.

REVISION HISTORY

Rev A Document (12/2007)
Initial release of this data sheet errata. Includes Data Sheet Clarifications 1 (Oscillator Configurations – PLL), 2 (Flash Program Memory), 3 (EUSART), 4 (A/D), 5 (Comparator), 6 (Comparator Voltage Reference), 7 (Special Features of the CPU) and 8 (Electrical Characteristics).

Rev B Document (9/2008)
Changes to Data Sheet Clarification 7 (Special Features of the CPU).

NOTES:

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