NCP81245

Three-Rail Output Controller with Single Intel Proprietary Interface for Desktop and Notebook CPU Applications

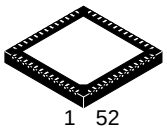
ON Semiconductor®

www.onsemi.com

The NCP81245 (3+3+1 phase) three−output buck solution is optimized for Intel's IMVP8 CPUs.

The two multi−phase rail control systems are based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing an ultra fast initial response to dynamic load events and reduced system cost.

The single−phase rail makes use of ON Semiconductor's patented high performance RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous−frequency−scaling operation and continuous−mode full−power operation. The NCP81245 has an ultra−low offset current monitor amplifier with programmable offset compensation for high−accuracy current monitoring.



QFN52
MN SUFFIX
CASE 485BE

MARKING DIAGRAM

F = Wafer Fab
A = Assembly Site
WL = Lot ID
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81245MNTXG	QFN52 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Three−Phase Rails Feature

- Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 300 kHz − 750 kHz
- Vin range 4.5 V to 20 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- UltraSonic Operation
- These Devices are Pb−Free and are RoHS Compliant

Single−Phase Rail Features

- Enhanced RPM Control System
- Ultra Low Offset IOUT Monitor
- Dynamic VID Feed−Forward
- Programmable Droop Gain
- Zero Droop Capable
- Thermal Monitor
- UltraSonic Operation
- Adjustable Vboot
- Digitally Controlled Operating Frequency

Applications

- Desktop & Notebook Processors
- Gaming

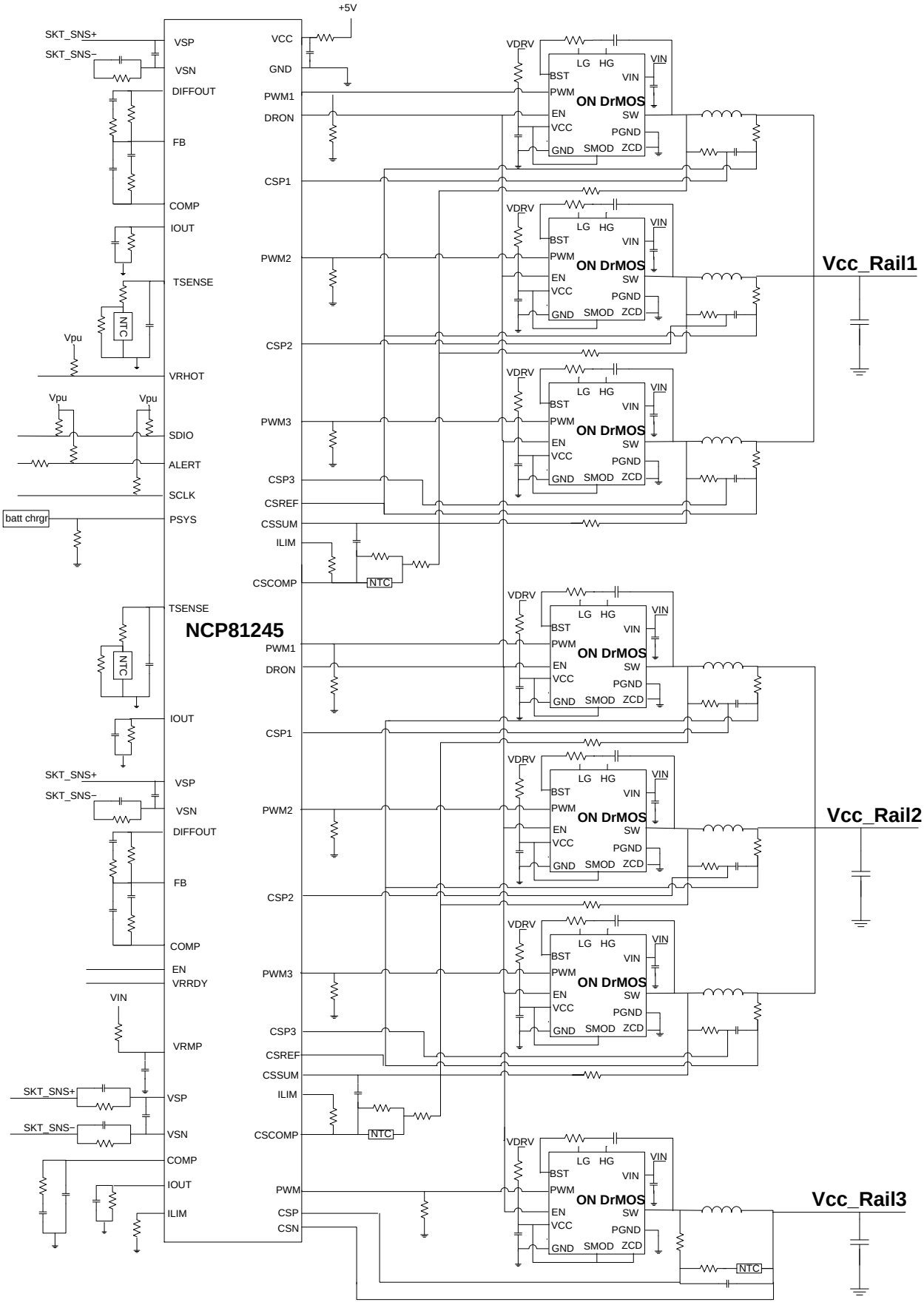

NCP81245
SKT_SNS+
SKT_SNS−
VSP
VSN
DIFFOUT
FB
COMP
IOUT
TSENSE
NTC
Vpu
VRHOT
SDIO
ALERT
SCLK
batt chrgr
PSYS
EN
VRRDY
VIN
VRMP
+5V
VCC
GND
PWM1
DRON
CSP1
PWM2
CSP2
PWM3
CSP3
CSREF
CSSUM
ILIM
CSCOMP
PWM
CSP
CSN
VDRV
LG
HG
BST
SW
PGND
SMOD
ZCD
ON DrMOS
Vcc_Rail1
Vcc_Rail2
Vcc_Rail3

Figure 1.

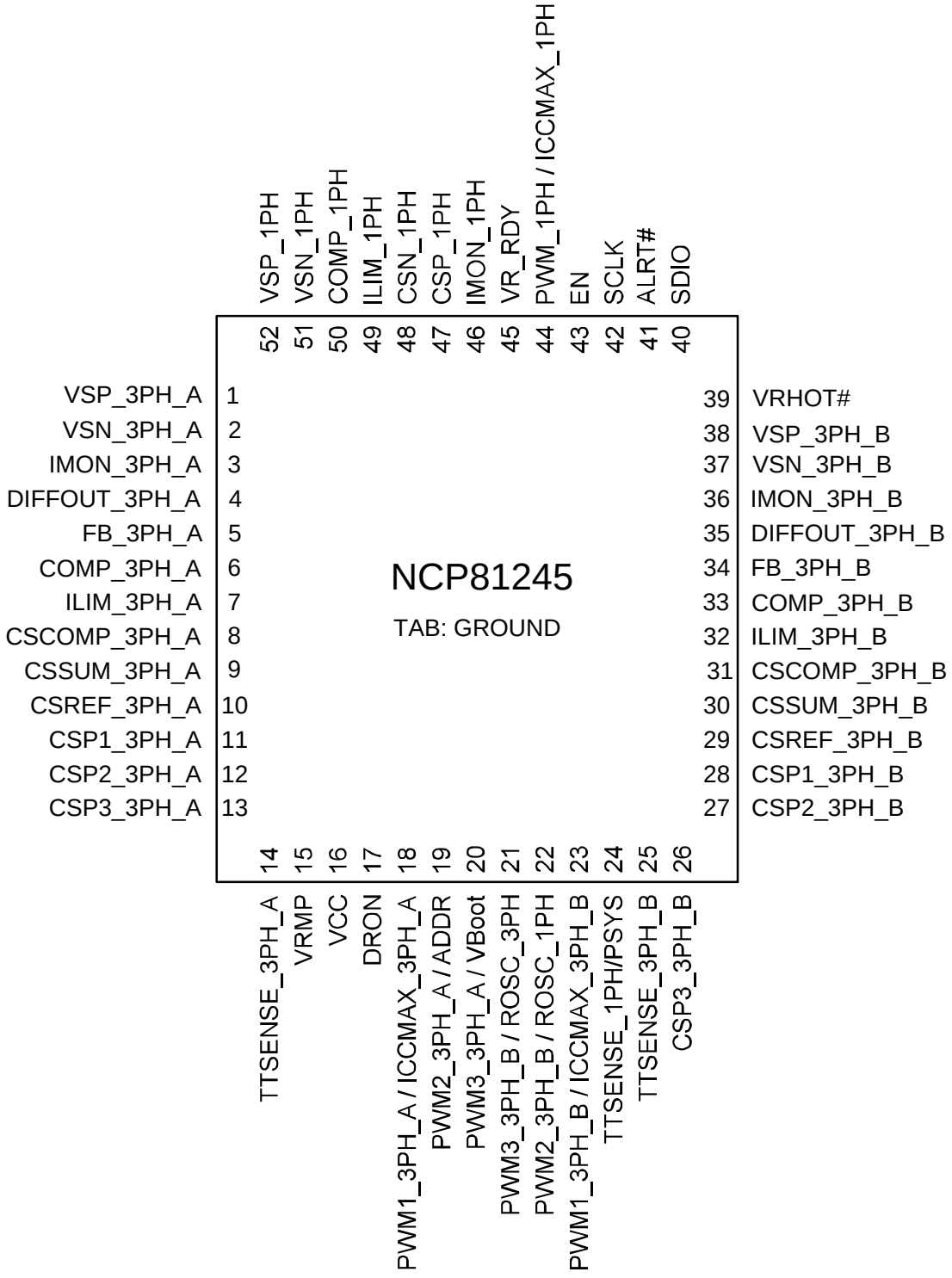


Figure 2. Pinout

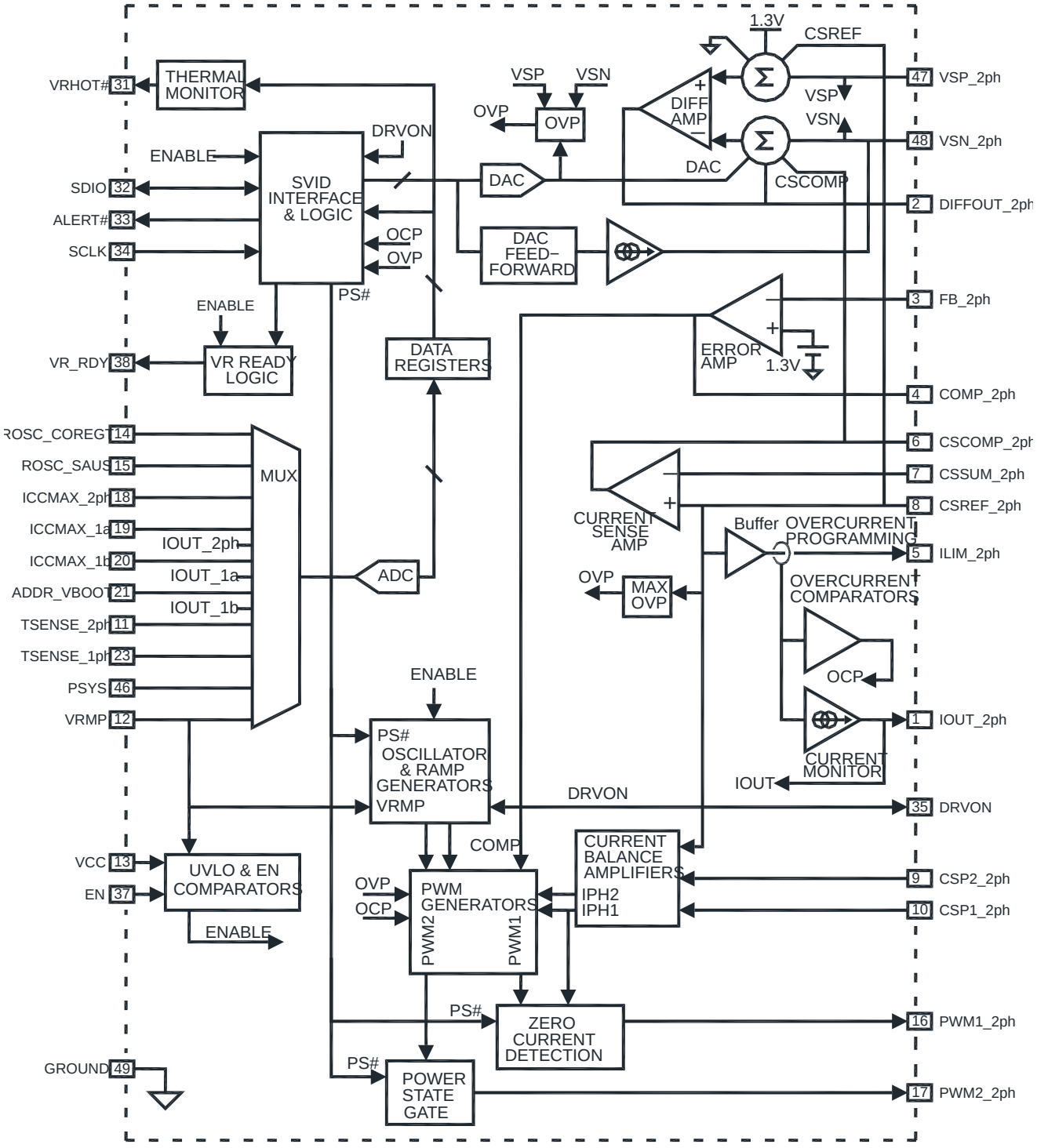


Figure 3. Block Diagram of Dual Edge Architecture

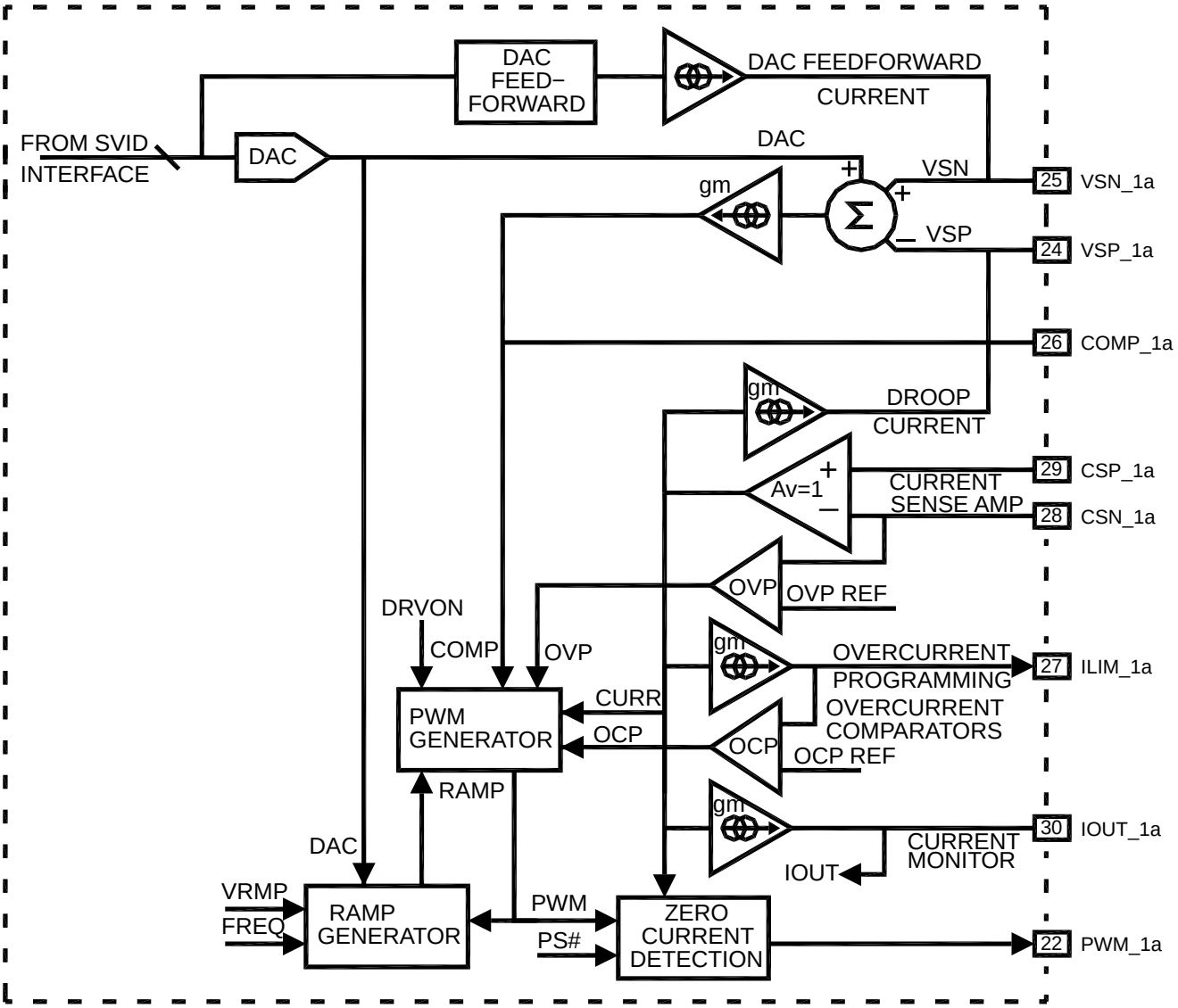


Figure 4. Block Diagram of Enhanced RPM Architecture

Table 1. QFN52 PIN LIST DESCRIPTION

Pin	Name	Description
1	VSP_3PH_A	Differential output voltage sense positive for multi−phase rail “A”
2	VSN_3PH_A	Differential output voltage sense negative for multi−phase rail “A”
3	IMON_3PH_A	A resistor to ground programs IOUT gain for multi−phase rail “A”
4	DIFFOUT_3PH_A	Output of multi−phase rail “A” differential remote sense amplifier
5	FB_3PH_A	Error amplifier voltage feedback for multi−phase rail “A”
6	COMP_3PH_A	Error amplifier output and PWM comparator inverting input for multi−phase rail “A”
7	ILIM_3PH_A	A resistor to CSCOMP_3PH_A programs the over−current threshold for multi−phase rail “A”
8	CSCOMP_3PH_A	Total−current−sense amplifier output for multi−phase rail “A”
9	CSSUM_3PH_A	Inverting input of total−current−sense amplifier for multi−phase rail “A”
10	CSREF_3PH_A	Total−current−sense amplifier reference voltage input for multi−phase rail “A”
11	CSP1_3PH_A	Current−balance amplifier positive input for Phase 1 of multi−phase rail “A”
12	CSP2_3PH_A	Current−balance amplifier positive input for Phase 2 of multi−phase rail “A”
13	CSP3_3PH_A	Current−balance amplifier positive input for Phase 3 of multi−phase rail “A”
14	TTSENSE_3PH_A	Temperature sense input for multi−phase rail “A”
15	VRMP	Vin feed−forward input. Controls a current used to generate the ramps of the modulators
16	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
17	DRON	External FET driver enable for discrete driver or DrMOS
18	PWM1_3PH_A / ICCMAX_3PH_A	Phase 1 PWM output of multi−phase rail “A” / A resistor to ground programs ICCMAX for multi−phase rail “A”
19	PWM2_3PH_A / ADDR	Phase 2 PWM output of multi−phase rail “A” / A resistor to ground configures Intel proprietary interface addresses for all 3 rails (ADDR)
20	PWM3_3PH_A / VBOOT	Phase 3 PWM output of multi−phase rail “A” / A resistor to ground configures boot voltage for all 3 rails (VBOOT)
21	PWM3_3PH_B / ROSC_3PH	Phase 3 PWM output of multi−phase rail “B” / Phase 4 PWM output of multi−phase rail “A” / A resistor to ground configures Fsw for both “A” and “B” multi−phase rails (ROSC_3PH)
22	PWM2_3PH_B / ROSC_1PH	Phase 2 PWM output of multi−phase rail “B” / A resistor to ground configures Fsw for 1ph rail (ROSC_1ph)
23	PWM1_3PH_B / ICCMAX_3PH_B	Phase 1 PWM output of multi−phase rail “B” / A resistor to ground programs ICCMAX for multi−phase rail “B”
24	TTSENSE_1PH / PSYS	Temperature sense input for the single−phase rail / System input power monitor. A resistor to ground scales this signal
25	TTSENSE_3PH_B	Temperature sense input for multi−phase rail “B”
26	CSP3_3PH_B	Current−balance amplifier positive input for Phase 3 of multi−phase rail “B” / Phase 4 of multi−phase rail “A”
27	CSP2_3PH_B	Current−balance amplifier positive input for Phase 2 of multi−phase rail “B”
28	CSP1_3PH_B	Current−balance amplifier positive input for Phase 1 of multi−phase rail “B”
29	CSREF_3PH_B	Total−current−sense amplifier reference voltage input for multi−phase rail “B”
30	CSSUM_3PH_B	Inverting input of total−current−sense amplifier for multi−phase rail “B”
31	CSCOMP_3PH_B	Total−current−sense amplifier output for multi−phase rail “B”
32	ILIM_3PH_B	A resistor to CSCOMP_3PH_B programs the over−current threshold for multi−phase rail “B”
33	COMP_3PH_B	Error amplifier output and PWM comparator inverting input for multi−phase rail “B”
34	FB_3PH_B	Error amplifier voltage feedback for multi−phase rail “B”
35	DIFFOUT_3PH_B	Output of multi−phase rail “B” differential remote sense amplifier
36	IMON_3PH_B	A resistor to ground programs IOUT gain for multi−phase rail “B”
37	VSN_3PH_B	Differential output voltage sense negative for multi−phase rail “B”

Table 1. QFN52 PIN LIST DESCRIPTION

Pin	Name	Description
38	VSP_3PH_B	Differential output voltage sense positive for multi−phase rail “B”
39	VR_HOT#	Thermal logic output for over−temperature condition on TTSENSE pins
40	SDIO	Serial VID data interface
41	ALERT#	Serial VID ALERT#
42	SCLK	Serial VID clock
43	EN	Enable input. High enables all three rails
44	PWM_1PH / ICCMAX_1PH	PWM output of the single−phase rail / A resistor to ground programs ICCMAX for the single−phase rail
45	VR_RDY	VR_RDY indicates all three rails are ready to accept Intel proprietary interface commands
46	IMON_1PH	A resistor to ground programs IOUT gain for the single−phase rail
47	CSP_1PH	Differential current sense positive for the single−phase rail
48	CSN_1ph	Differential current sense negative for the single−phase rail
49	ILIM_1ph	A resistor to ground programs ILIM gain for the single−phase rail
50	COMP_1ph	Compensation for single−phase rail
51	VSN_1ph	Differential output voltage sense negative for single−phase rail
52	VSP_1ph	Differential output voltage sense positive for single−phase rail
53	Tab	GND

ELECTRICAL INFORMATION

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMPX	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMPX	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VSN	GND + 300 mV	GND−300 mV	1 mA	1 mA
VRDY	VCC + 0.3 V	−0.3 V	N/A	2 mA
VCC	6.5 V	−0.3 V	N/A	N/A
VRMP	+25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to GND unless noted otherwise.

Table 3. THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 1)	R_{JA}	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to +125	°C
Operating Ambient Temperature Range		−40 to +100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. 2) JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. 3) JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V ; C_{VCC} = 0.1μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current		−900		900	nA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 kΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 0.75 V − 1.52 V, CL = 20 pF to GND, DC Load = 10k to GND		5		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5			V
Minimum Output Voltage	I_{SINK} = 2.0 mA			1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−25		25	nA
VSP Input Voltage Range		−0.3		3.0	V
VSN Input Voltage Range		−0.3		0.3	V
−3dB Bandwidth	CL = 20 pF to GND, RL = 10 k Ω to GND		22.5		MHz
Closed Loop DC gain VS to DIFF	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.5			V
Minimum Output Voltage	I_{SINK} = 2 mA			0.8	V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		−300		300	μV
Input Bias Current	CSREF= 1 V	−7.5		7.5	μA
Input Bias Current	CSSUM= 1 V	−7.5		7.5	nA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		15		MHz
Maximum CSCOMP (A) Output Voltage	Isource = 2 mA	3.5			V
Minimum CSCOMP(A) Output Voltage	Isink = 500 uA			0.15	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSPX − CSPX + 1 = 1.2 V	−50		50	nA
Common Mode Input Voltage Range	CSPx = CSREF	0		2.3	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100		100	mV
Closed loop Input Offset Voltage Matching	CSPx = 1.2 V, Measured from the average	−1.5		1.5	mV
Current Sense Amplifier Gain	0V < CSPx < 0.1 V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSREF = CSP = 10 mV to 30 mV	−3		3	%
−3dB Bandwidth			8		MHz
BIAS SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	Enable high		33	50	mA
VCC Quiescent Current	Enable low			60	μA

Table 4. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V ; C_{VCC} = 0.1μF

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			
VCC UVLO Hysteresis			250		mV
VRMP					
Supply Range		4.5		20	V
UVLO Threshold	VRamp rising			4.25	V
	VRamp falling	3			V
UVLO Hysteresis			675		mV
DAC SLEW RATE					
Slew Rate Fast			>10		mV/μs
Soft Start Slew Rate			1/2 SR Fast		mV/μs
Slew Rate Slow			1/2 SR Fast		mV/μs
ENABLE INPUT					
Enable High Input Leakage Current	Enable = 0	−1		1	μA
V_{IH}		0.8			V
V_{IL}				0.3	V
Enable Delay Time	Measure time from Enable transitioning HI , VBOOT is not 0 V			2.5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0			V
Output Low Voltage	Sinking 500 μA			0.1	V
Pull Up Resistances			2.0		kΩ
Rise/Fall Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		160		ns
Internal Pull Down Resistance	V_{CC} = 0 V		70		kΩ
OVERCURRENT PROTECTION					
Ilim Threshold Current (delayed OCP shutdown)	PS0	9	10	11	μA
	PS1, PS2, PS3 (N = PS0 phase count)		10/N		
Ilim Threshold Current (immediate OCP shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3 (N = PS0 phase count)		15/N		
Shutdown Delay	Immediate		300		ns
	Delayed		50		μs
ILIM Output Voltage Offset	Ilim sourcing 10 μA	−2		2	mV
IOUT_3PH_A/IOUT_3PH_B OUTPUT					
Output Offset Current	V_{Ilim} = 5 V			0.25	μA
Output current max	Ilimit sink current 20 μA		200		μA
Current Gain	(Iout current)/(Ilimit Current) Rlim = 20k, Riout = 5k DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	A/A

Table 4. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V ; C_{VCC} = 0.1μF

Parameter	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR					
Switching Frequency Range		300		1200	kHz
Switching Frequency Accuracy	300 kHz < Fsw < 1 MHz	−10		10	%
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start		1.9	2.0	2.1	V
Over Voltage Threshold Above DAC	VSP rising	370	400	430	mV
Over Voltage Delay	VSP rising to PWMx low		25		ns
Under Voltage Threshold Below DAC−DROOP	VSP falling	225	300	370	mV
Under−voltage Hysteresis	VSP rising		25		mV
Under−Voltage Delay			5		μs
MODULATORS (PWM COMPARATORS) FOR A RAIL & B RAIL					
Minimum Pulse Width	Fsw = 350 kHz		40		ns
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP=12.0V		2.5		V
PWM Phase Angle Error	Between adjacent phases		±5		°
TSENSE					
VRHOT Assert Threshold			468		mV
VRHOT Rising Threshold			488		mV
Alert Assertion Threshold			488		mV
Alert Rising Threshold			510		mV
TSENSE Bias Current		115	120	125	μA
VRHOT					
Output Low Saturation Voltage	I_{VR_HOT} = −4 mA			0.3	V
Output Leakage Current	High Impedance State	−1		1	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1		1	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			+/−1		%
Conversion Time			7.4		μs
Round Robin			206		μs
VRDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA			0.3	V
Rise Time	External pull−up of 1 kΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 10% to 90%			150	ns
Fall Time	External pull−up of 1 KΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 90% to 10%			150	ns
Output Leakage Current When High	VR_RDY = 5.0 V	−1		1	μA
VR_RDY Delay (falling)	Due to OCP or OVP		0.3		μs

Table 4. ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V ; C_{VCC} = 0.1μF

Parameter	Test Conditions	Min	Typ	Max	Unit
PWM OUTPUTS					
Output High Voltage	Sourcing 500 μA	V_{CC} − 0.2			V
Output Mid Voltage	No Load	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA			0.3	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo =10% to 90% of VCC		5		ns
Tri−State Output Leakage	Gx = 2.0 V, x = 1−2, EN = Low	−1		1	μA
PHASE DETECTION					
CSPX Phase Disable Voltage		4.75			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SINGLE PHASE ELECTRICAL TABLE FOLLOWS

Table 5. ELECTRICAL CHARACTERISTICS Unless otherwise stated: −40°C<T_A<100°C; 4.75V<VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current		−25		25	nA
VSP Input Voltage Range		−0.3		3.0	V
VSN Input Voltage Range		−0.3		0.3	V
gm		1.344	1.6	1.856	mS
Output Offset Current		−15		15	μA
Open loop Gain	Load = 1 nF in series with 1 kΩ in parallel with 10 pF to ground	70	73		dB
Source Current	Input Differential −200 mV		280		μA
Sink Current	Input Differential 200 mV		280		μA
−3dB Bandwidth	Load = 1 nF in series with 1 kΩ in parallel with 10 pF to ground		20		MHz
IOUT					
CSP−CSN = 20 mV		0.97	1	1.03	mS
Output Offset Current	CSP = CSN	−200		200	nA
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start			2.0		V
Over Voltage Threshold Above DAC	VSP−VSN−VID setting	370		430	mV
Over Voltage Delay	VSP rising to PWMx low		25		ns
Over Voltage VR_RDY Delay	VSP rising to VR_RDY low		350		ns
Under Voltage Threshold	VSP−VSN falling	215	300	385	mV
Under−voltage Hysteresis	VSP−VSN falling/rising		25		mV
Under−voltage Blanking Delay	VSP−VSN falling to VR_RDY falling		5		μs
DROOP					
CSP−CSN − 20 mV		0.96	1	1.04	mS
Output Offset Current	CSP = CSN	−1.5		1.5	μA
OVERCURRENT PROTECTION					
ILIMIT Threshold		1.275	1.3	1.325	V
ILIMIT Delay			200		ns
ILIMIT Gain	CSP−CSN = 20 mV	0.925	1	1.075	mS
CSP−CSN ZCD comparator					
Offset Accuracy			±1.5		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

General

The NCP81245 is a three rail 3+3+1 phase PWM controller with a single serial Intel proprietary interface control interface.

Serial VID

For Intel proprietary interface communication details please contact Intel®, Inc.

NCP81245 Configurations

The NCP81245 has four Configuration pins that are secondary−functions on PWM pins. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- Intel proprietary interface address
  - For Intel proprietary interface address selection please see Table below.
  - For more information regrading Intel proprietary interface addresses please contact Intel, Inc.
- Phase doubler
  - The multi−phase A rail can use a Phase Doubler from ON Semiconductor.
  - Options to enable doubling on the A rail is provided in the Vboot configuration table
- Switching Frequency
  - Both multi−phase rails' per−phase switching frequency will be the same programmable value.
  - The 1−phase Fsw is programmed independently
  - The Fsw values are shown in the ROSC table
- Vboot
  - Addresses 00h, 01h, and 03 POR Vboot is 0V.
  - Address 02h POR Vboot is 1.05V
  - Vboot options are shown in the VBOOT table

Boot Voltage

Vboot for the NCP81245 is externally programmed using a single resistor.

See Vboot pin voltages and the corresponding Vboot level in the table below. During startup, the pin voltage is measured. This value cannot be changed after the initial power up sequence is complete.

Table 6. VBOOT PIN 20 CONFIGURATION

Resistor	3PH_A VBOOT	3PH_B VBOOT	1PH VBOOT	Rail A Doubler
6.19 kΩ	0 V	0 V	0 V	No
14.7 kΩ	0 V	0 V	0 V	Yes
24.9 kΩ	0 V	0 V	1.05 V	No
37.4 kΩ	0 V	0 V	1.05 V	Yes
53.6 kΩ	0 V	0 V	0.95 V	No
73.2 kΩ	0 V	0 V	0.95 V	Yes
97.6 kΩ	0 V	0 V	0.8 V	No
130 kΩ	0 V	0 V	0.8 V	Yes
169 kΩ	1.05 V	1.05 V	1.05 V	No
215 kΩ	1.05 V	1.05 V	1.05 V	Yes

Table 7. INTEL PROPRIETARY INTERFACE ADDRESS PIN 19 CONFIGURATION

Pull−Down Resistor	Slew Rate mV/µs	3PH_A Address	3PH_B Address	1PH Address	Pin 24 TSENSE/ PSYS	A max Phases	B max Phases
NCP81245 (3+3+1, Pin 21 = PWM3_3PH_B, Pin 26 = CSP3_3PH_B)							
4.3 kΩ	30	00h	01h	02h	PSYS	3	3
12.1 kΩ		00h	01h	03h	TSENSE	3	3
19.6 kΩ		01h	00h	02h	PSYS	3	3
31.6 kΩ		01h	00h	03h	TSENSE	3	3
49.9 kΩ	10	00h	01h	02h	PSYS	3	3
78.7 kΩ		00h	01h	03h	TSENSE	3	3
121 kΩ		01h	00h	02h	PSYS	3	3
174 kΩ		01h	00h	03h	TSENSE	3	3

PSYS

The PSYS pin is an analog input to the NCP81245. It is a system input power monitor that facilitates the monitoring of the total platform system power. For more information regarding PSYS please contact Intel, Inc.

Remote Sense Amplifier (multiphase)

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \left(V_{DROOP} - V_{CSREF}\right) \quad \text{(eq. 1)}$$

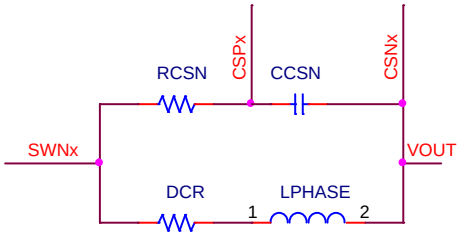
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier (multiphase)

A high performance error amplifier is provided for high bandwidth transient performance. A standard type III compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers (multiphase)

Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSPx pins are high impedance inputs. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

Figure 5.

Total Current Sense Amplifier (multiphase)

The NCP81245 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

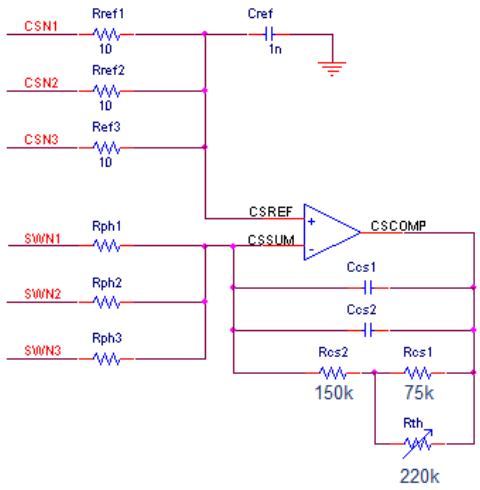


Figure 6.

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{Total} * DCR\right) \quad \text{(eq. 2)}$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 220k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25^\circ C}{2 * PI * L_{Phase}} \quad \text{(eq. 3)}$$

Programming the Current Limit (multiphase)

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

$$R_{LIMIT} = \frac{\frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{LIMIT} * DCR\right)}{10\mu} \quad \text{(eq. 4)}$$

or

$$R_{LIMIT} = \frac{V_{CSCOM-CSREF@ILIMIT}}{10\mu} \quad \text{(eq. 5)}$$

Programming DAC Feed−Forward Filter (multiphase)

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.

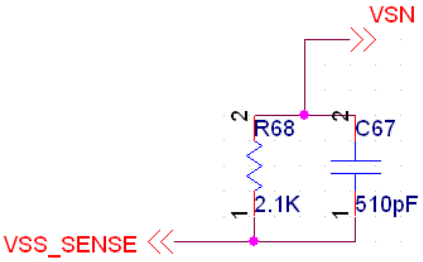


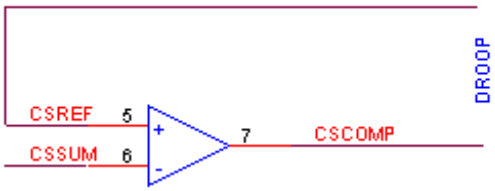
Figure 7.

$$Rvsn = Cout * Rout * 453.6 \times 10^6 \quad \text{(eq. 6)}$$

$$Cvsn = \frac{Rout * Cout}{Rvsn} \quad \text{(eq. 7)}$$

Programming DROOP (multiphase)

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



$$Droop = DCR * (Rcs/Rph)$$

Figure 8.

Programming IOUT (multiphase)

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A

pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2\ V * R_{LIMIT}}{10 * \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{ICC\_MAX} * DCR\right)} \quad \text{(eq. 8)}$$

Programming ICC_MAX (multiphase)

A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10k.

$$ICC\_MAX_{21k} = \frac{R * 10\ \mu A * 256\ A}{2\ V} \quad \text{(eq. 9)}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.

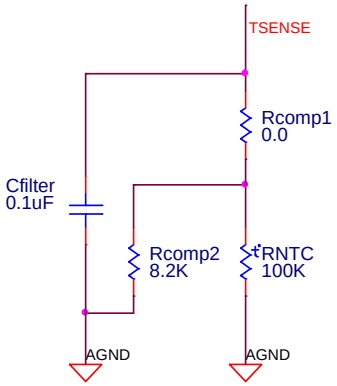


Figure 9.

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 300 kHz/phase to 1.2 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

Table 8. 3 PHASE / 1 PHASE FSW V ROSC (PIN21 / PIN22)

Resistor	Per phase Fsw MPH_A	Per phase Fsw MPH_B	Per phase Fsw 1PH
6.19 kΩ	1.2 MHz	1.2 MHz	1.2 MHz
14.7 kΩ	1.1 MHz	1.1 MHz	1.1 MHz
24.9 kΩ	1.0 MHz	1.0 MHz	1.0 MHz
37.4 kΩ	900 kHz	900 kHz	900 kHz
53.6 kΩ	800 kHz	800 kHz	800 kHz
73.2 kΩ	700 kHz	700 kHz	700 kHz
97.6 kΩ	600 kHz	600 kHz	600 kHz
130 kΩ	500 kHz	500 kHz	500 kHz
169 kΩ	400 kHz	400 kHz	400 kHz
215 kΩ	300 kHz	300 kHz	300 kHz

The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the single phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

For use with ON Semiconductor's phase doubler, the NCP81245 offers the user the ability to multiply the frequency of multiphase rail A. On the NCP81245, the switching frequency is increased by a factor of 2 when the phase doubler configuration is used.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following,

$$V_{RAMPpk=pkPP} = 0.1 * V_{VRMP} \quad \text{(eq. 10)}$$

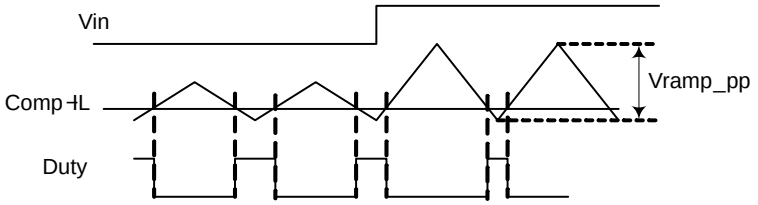


Figure 10.

PWM Comparators

The non−inverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (IL*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

PHASE DETECTION SEQUENCE

The NCP81245 normally operates as a 3−ph Vcc_Rail1 + 3−ph Vcc_Rail2 + 1−ph Vcc_Rail3. Phases of the multi−phase rails can be disabled by pulling up CSP pins to VCC.

For example, to configure one of the 3 phase rails of the NCP81245 as a 1 phase rail, CSP2 and CSP3 of that rail must be pulled up to Vcc on startup.

Both the single−phase rails and multi−phase rail B can be disabled by pulling all of their associated CSP pins to Vcc. Phase 1 of multi−phase rail A cannot be disabled.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers or DrMOS. As each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

PROTECTION FEATURES

Under voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81245 monitors the 5 V V_{CC} supply. The gate driver monitors both the gate driver V_{CC} and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off its startup sequence. In this case the PWM is set to the MID state to begin soft start.

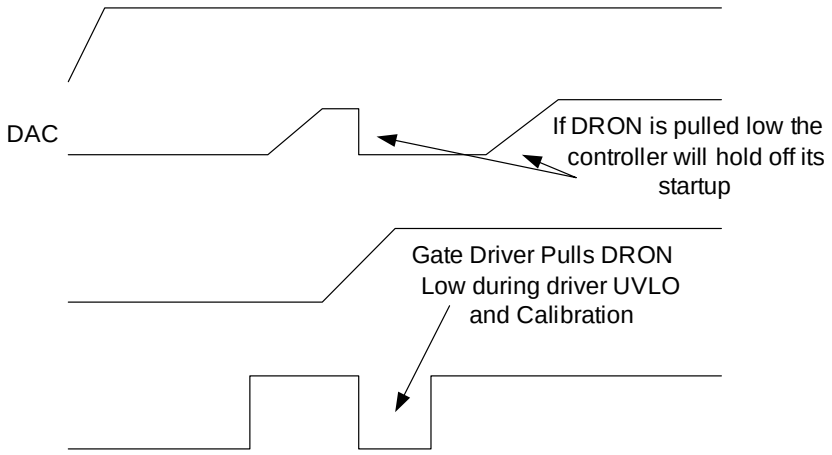


Figure 11. Gate Driver UVLO Restart

Soft−start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected, if the controller is enabled the PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state.

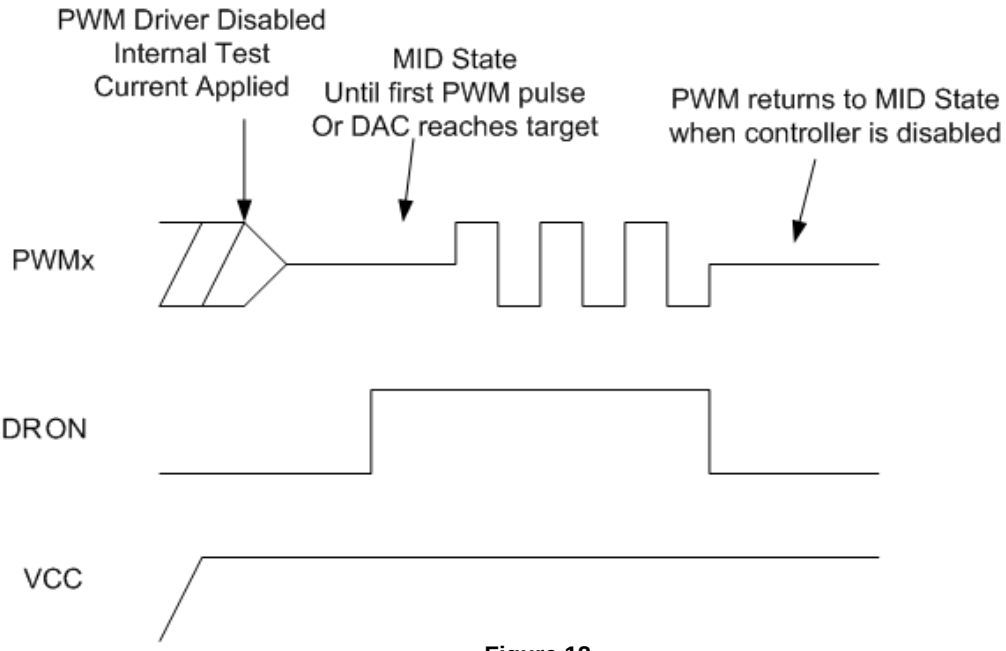


Figure 12.

Over Current Latch− Off Protection (multiphase)

The NCP81245 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs(shut down immediately for 150% load current) after which the outputs will remain disabled until the V_{CC} voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations,

Equation related to the NCP81245 multiphase rails:

$$R_{ILIM} = \frac{I_{LIM} * DCR * Rcs/Rph}{I_{CL}} \qquad \text{(eq. 11)}$$

Where I_{CL} = 10 μA

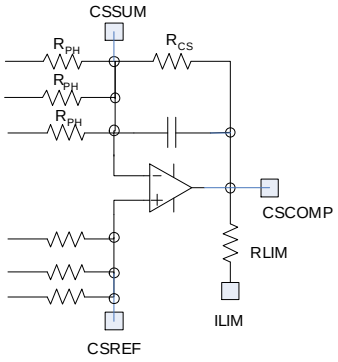


Figure 13.

Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low. The 300 mV limit can be reprogrammed using the VR_Ready_Low Limit register.

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V. The part will stay in this mode until the V_{CC} voltage or EN is toggled

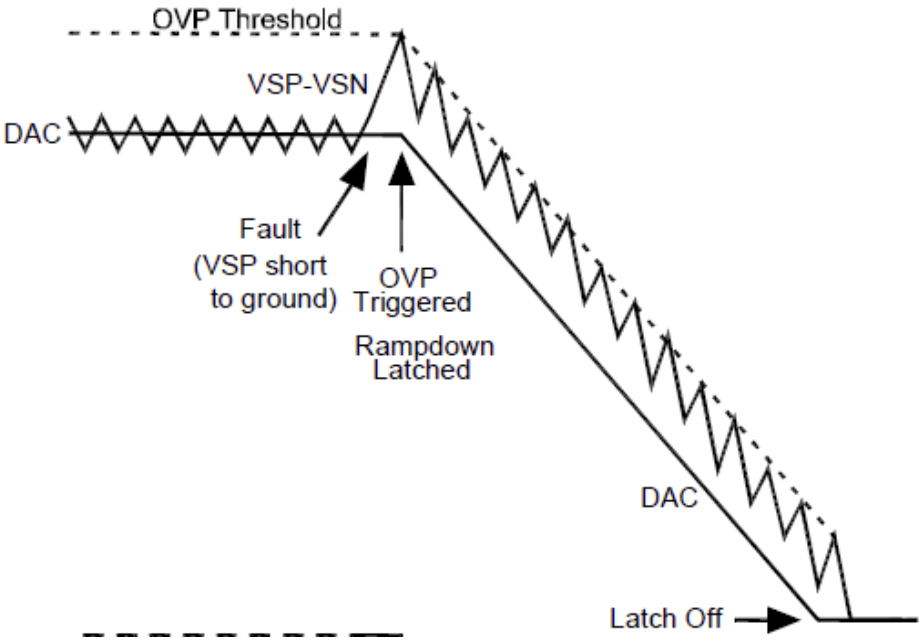


Figure 14.

OVP During Normal Operation Mode

During start up, the OVP threshold is set to 2.0 V. This allows the controller to start up without false triggering the OVP.

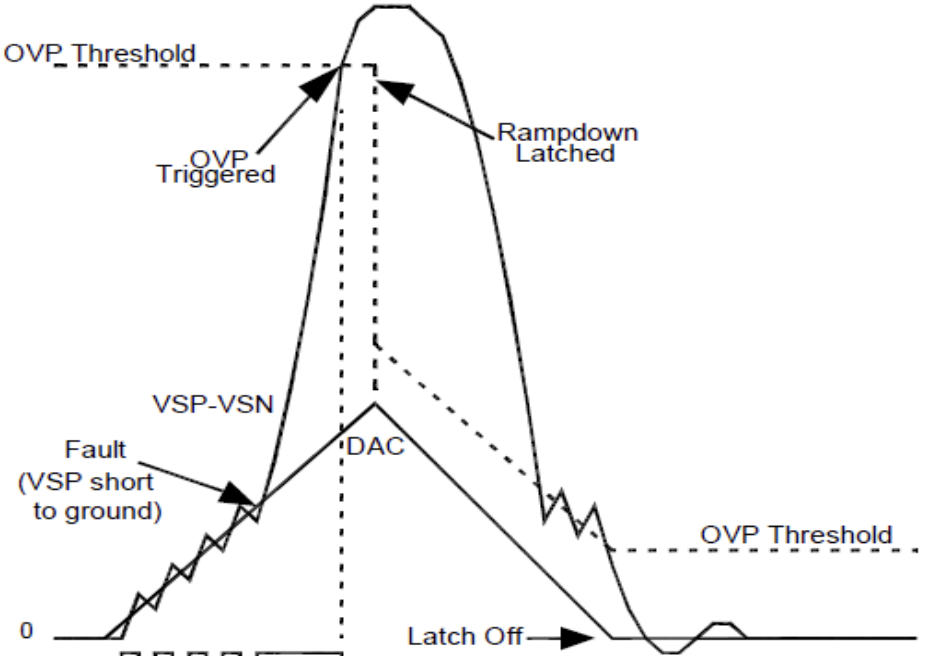


Figure 15. OVP Behavior at Startup

Single−Phase Rail

The architecture of the single−phase rail makes use of a digitally enhanced, high performance, current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions. At light load the single−phase rail automatically transitions into DCM operation to save power.

Single−phase Rail Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks described in the following Droop section and the DAC Feedforward filter section. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm \times \left[V_{DAC} - \left(V_{VSP} - V_{VSN}\right)\right] \quad \text{(eq. 12)}$$

This current is applied to a standard Type II compensation network.

Single−phase rail voltage compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF.

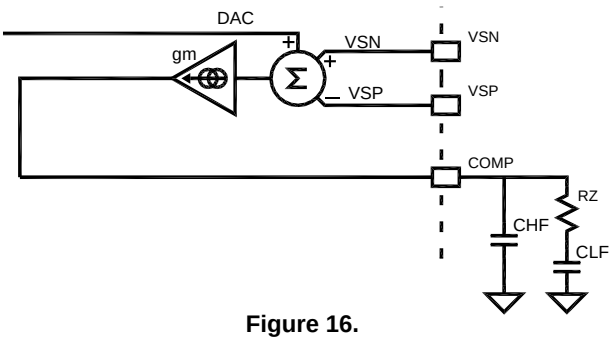


Figure 16.

Single−phase Rail − Differential Current Feedback Amplifier

The single−phase controller has a low offset, differential amplifier to sense output inductor current. An external lowpass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The lowpass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_Z = \frac{DCR@25^\circ C}{2 * \pi * L} \quad \text{(eq. 13)}$$

$$F_P = \frac{1}{2 * \pi * \left(\frac{R_{PHSP} * \left(Rth + R_{CSSP} \right)}{R_{PHSP} + Rth + R_{CSSP}} \right) * C_{CSSP}} \quad \text{(eq. 14)}$$

Forming the lowpass filter with an NTC thermistor (Rth) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of R_{PHSP} and R_{CSSP} are set based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the lowpass filter resistance not exceed 10 kΩ in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 mΩ for sufficient current accuracy. Recommended values for the external filter components are:

$$C_{CSSP} = \frac{L_{PHASE}}{\frac{R_{PHSP} * \left(Rth + R_{CSSP} \right)}{R_{PHSP} + Rth + R_{CSSP}} * DCR} \quad \text{(eq. 15)}$$

R_{PHSP} = 7.68 kΩ
R_{CSSP} = 14.3 kΩ
Rth = 100 kΩ, Beta = 4300

Using 2 parallel capacitors in the lowpass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} * Iout * DCR \quad \text{(eq. 16)}$$

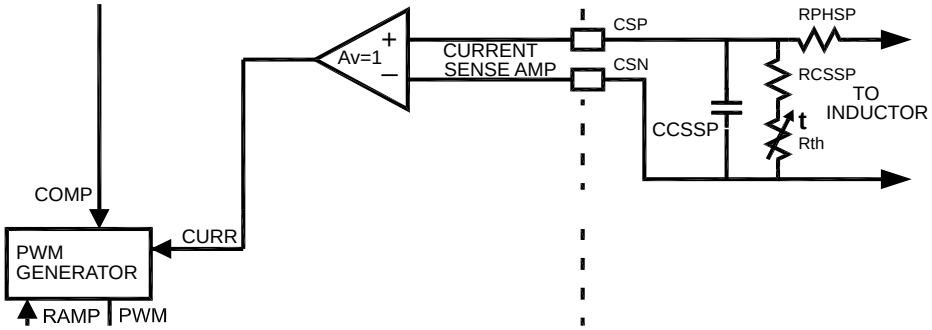
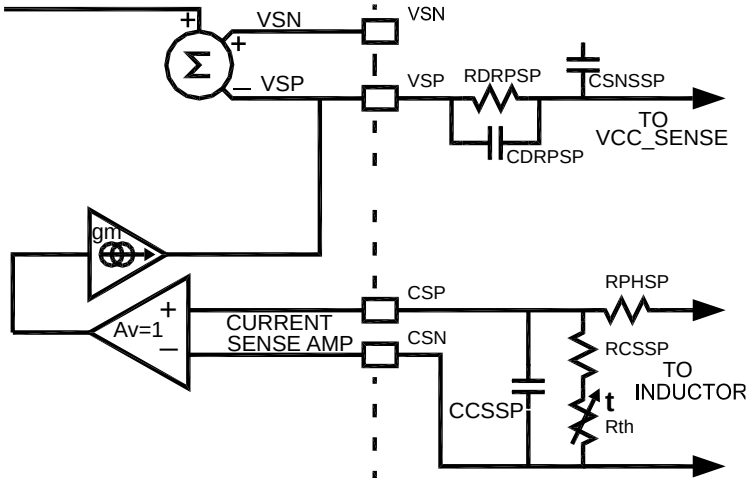


Figure 17.

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

Single−phase Rail − Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP}, proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81245, a loadline is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal − thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.



$$V_{DROOP} = R_{DRPSP} \times gm \times \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} \times I_{OUT} \times DCR$$

Figure 18.

The loadline is programmed by choosing R_{DRPSP} such that the ratio of voltage produced across R_{DRPSP} to output current is equal to the desired loadline.

$$R_{DRPSP} = \frac{Loadline}{gm \times DCR} \times \frac{R_{PHSP} + Rth + R_{CSSP}}{Rth + R_{CSSP}} \quad \text{(eq. 17)}$$

Single−phase Rail − Programming the DAC Feed−Forward Filter

The DAC feed−forward implementation for the single−phase rail is the same as for the multi−phase rails. The NCP81245 outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. RFFSP sets the gain of the DAC feed−forward and CFFSP provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance of the system.

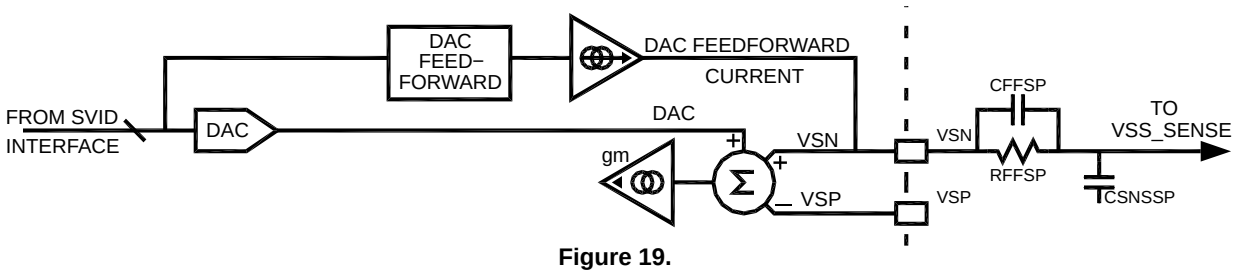


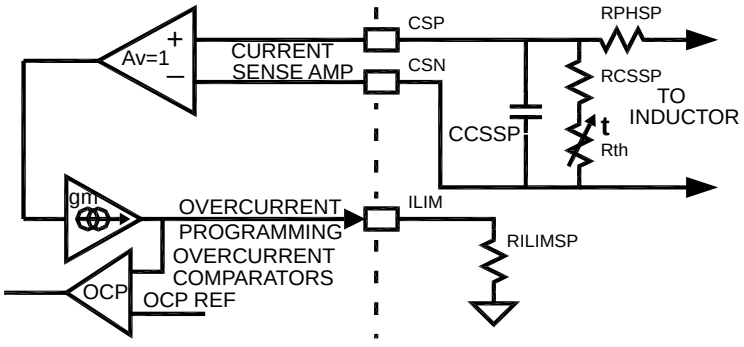
Figure 19.

$$R_{FFSP} = \frac{Loadline * Cout}{1.35\ nF} \quad \text{(eq. 18)}$$

$$C_{FFSP} = \frac{200\ ns}{R_{FFSP}} \quad \text{(eq. 19)}$$

Single−phase Rail − Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIMSP}) from the ILIM pin to ground. The current limit latches the single−phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the current limit resistor based on the equation shown below. A capacitor can be placed in parallel with the programming resistor to slightly delay activation of the latch if some tolerance of short overcurrent events is desired.



$$R_{ILIMSP} = \frac{1.3\ V}{gm \cdot \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} \times Iout_{LIMIT} \times DCR}$$

Figure 20.

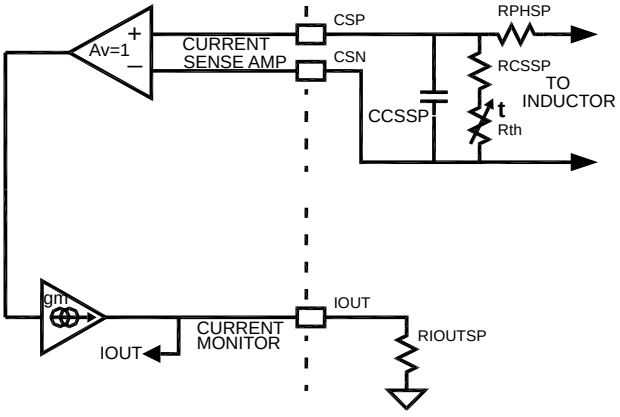
When selecting the current limit it is necessary to take into account the additional inductor current due to the slew rate of the output voltage across the output capacitance during VID changes, as this excess current may cause the OCP limit to be exceeded. This excess current is given by:

$$I = Cout \times \times \frac{dVout}{dt} \qquad \text{(eq. 20)}$$

where $\frac{dVout}{dt}$ is the maximum slew rate

Single−phase Rail − Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if needed.



$$R_{IOUTSP} = \frac{2\ V}{gm \times \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} \times IccMax \times DCR}$$

Figure 21.

Single−phase Rail PWM Comparators

The non−inverting input of each comparator (one for each phase) is connected to the summation of the output of the error amplifier (COMP) and each phase current (I_L*DCR*Phase Current Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output.

A PWM pulse starts when the error amp signal (COMP voltage) rises above the trigger threshold plus gained−up inductor current, and stops when the artificial ramp plus gained−up inductor current crosses the COMP voltage. Both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the COMP voltage increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

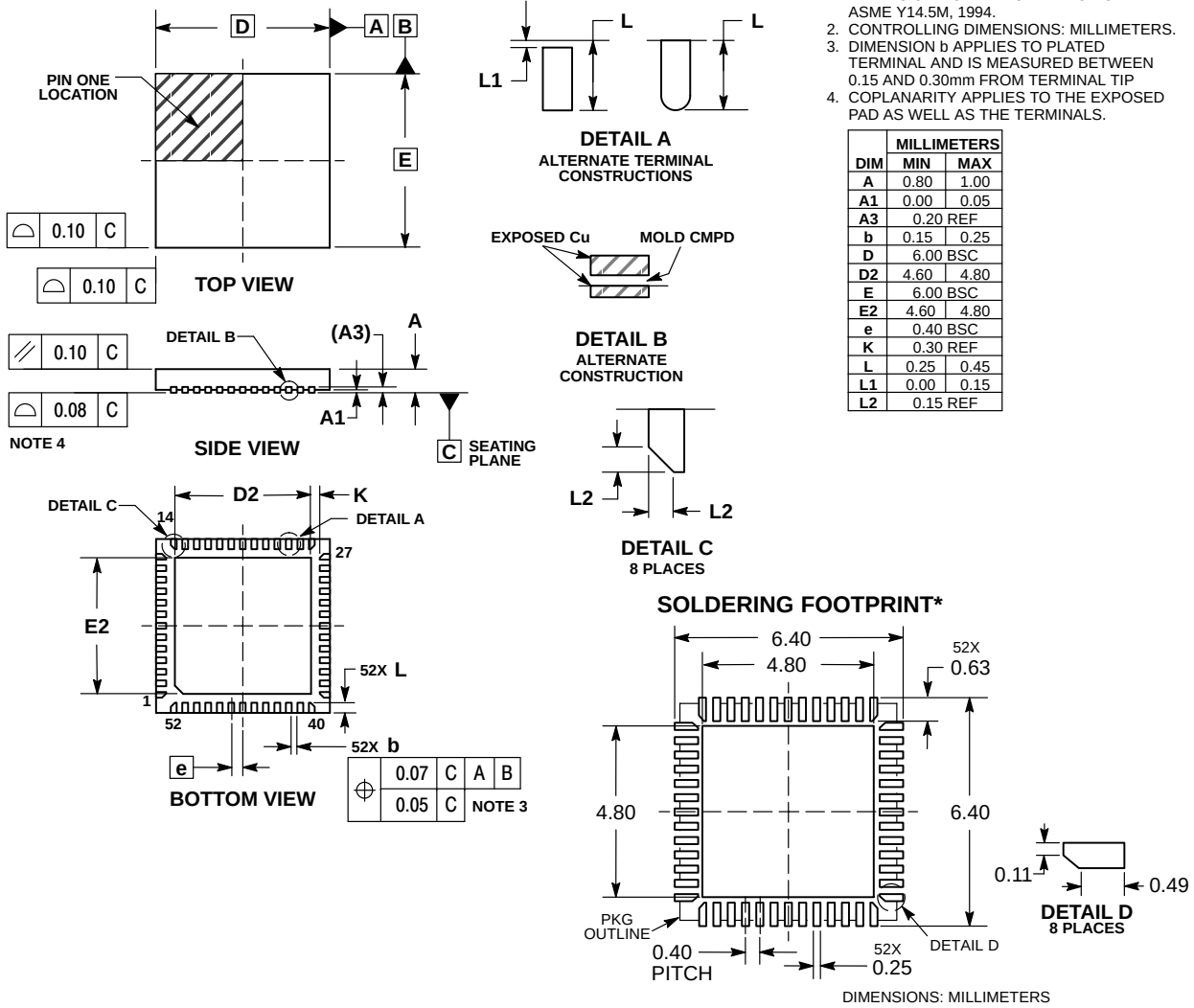
Programming ICC_MAX (single phase)

A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10k.

$$ICC\_MAX_{21h} = \frac{R\,max * 10\ \mu A * 256\ A}{4 * 2\ V} \qquad \text{(eq. 21)}$$

PACKAGE DIMENSIONS

QFN52 6x6, 0.4P
CASE 485BE
ISSUE B



DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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