

P-channel 40 V, 0.0125 Ω typ., 10 A, StripFET™ F6 Power MOSFET in SO-8 package

Datasheet - production data

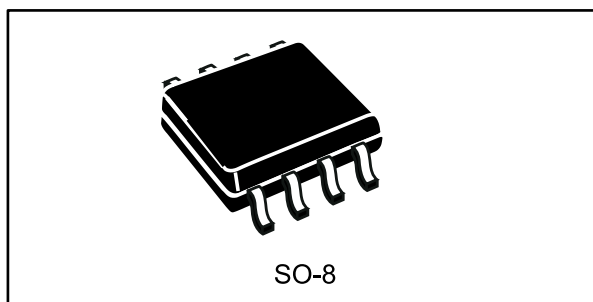
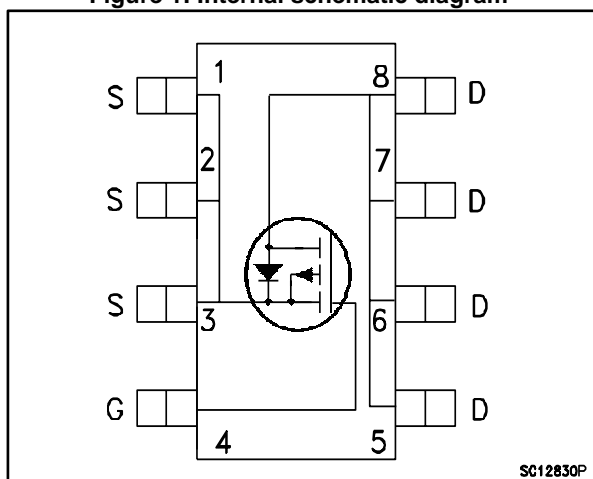


Figure 1: Internal schematic diagram



- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the StripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STS10P4LLF6	10K4L	SO-8	Tape and reel

-  For the P-channel MOSFET actual polarity of voltages and current have to be reversed

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS10P4LLF6	40 V	0.015	10 A

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ }^{\circ}\text{C}$	10	A
I_D	Drain current (continuous) at $T_{amb} = 100\text{ }^{\circ}\text{C}$	5.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{amb} = 25\text{ }^{\circ}\text{C}$	2.7	W
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature	150	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	47	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10$ sec



For the P-channel MOSFET actual polarity of voltages and current have to be reversed

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA	40			V V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 40 V			1	μA
		V _{DS} = 30 V, T _C = 125 °C			10	
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1			V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3 A		0.0125	0.015	Ω
		V _{GS} = 4.5 V, I _D = 3 A		0.017	0.02	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	3525	-	pF
C _{oss}	Output capacitance		-	344	-	pF
C _{rss}	Reverse transfer capacitance		-	238.5	-	pF
Q _g	Total gate charge	V _{DD} = 20 V, I _D = 10 A V _{GS} = 4.5 V	-	34	-	nC
Q _{gs}	Gate-source charge		-	11.3	-	nC
Q _{gd}	Gate-drain charge		-	13.8	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 20 V, I _D = 5 A R _G = 4.7 Ω V _{GS} = 10 V	-	49.4	-	ns
t _r	Rise time			60.6		
t _{d(off)}	Turn-off delay time			170		
t _f	Fall time			20		



For the P-channel MOSFET actual polarity of voltages and current have to be reversed

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 3 \text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 10 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	29		ns
Q_{rr}	Reverse recovery charge		-	27.6		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel MOSFET actual polarity of voltages and current have to be reversed

3 Electrical characteristics (curves)

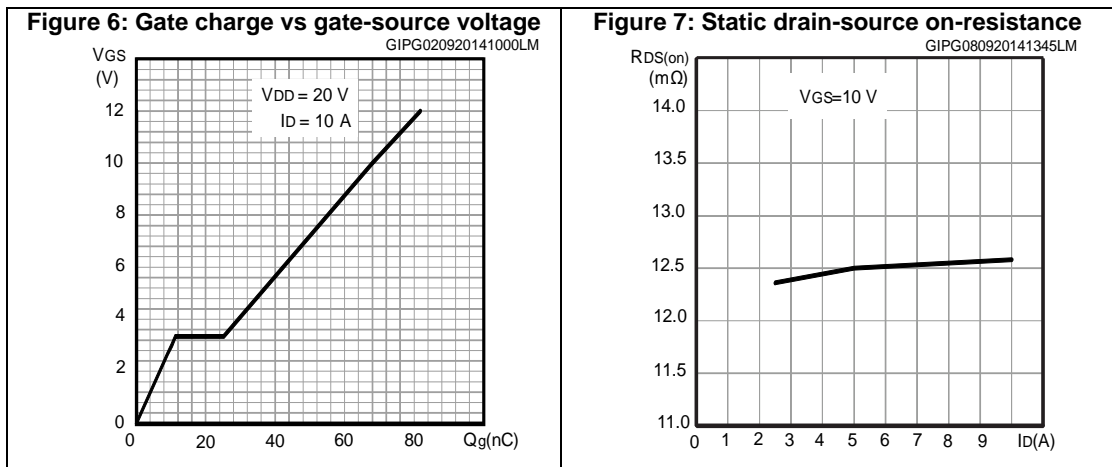
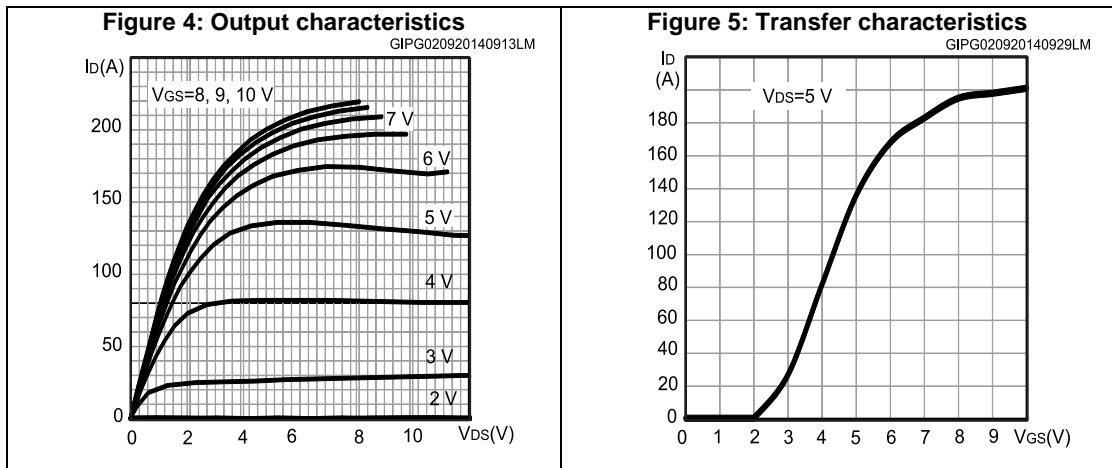
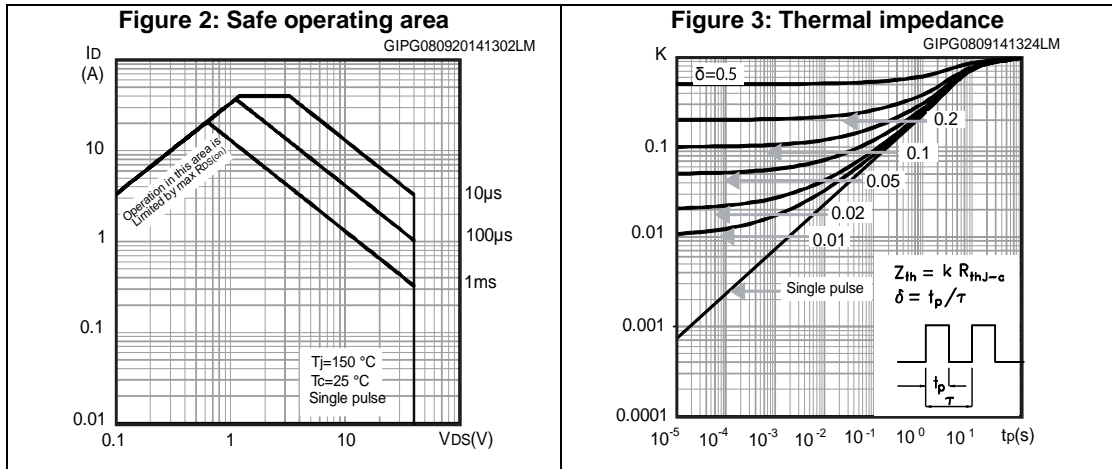


Figure 8: Capacitance variation

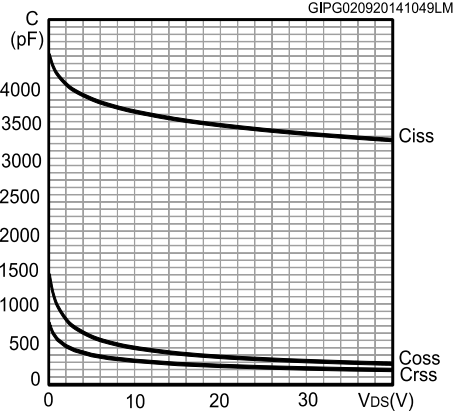


Figure 9: Normalized gate threshold voltage vs temperature

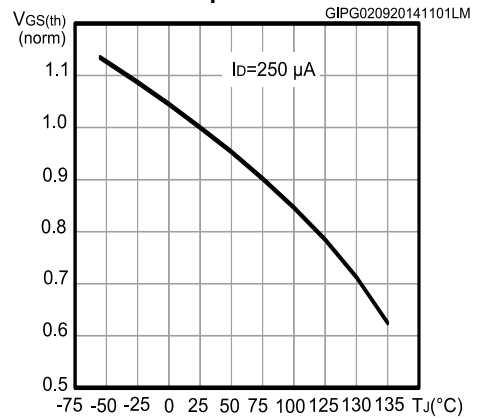


Figure 10: Normalized on-resistance vs temperature

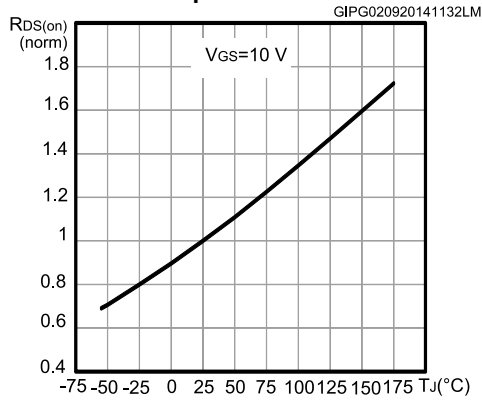


Figure 11: Normalized VBR(DSS) vs temperature

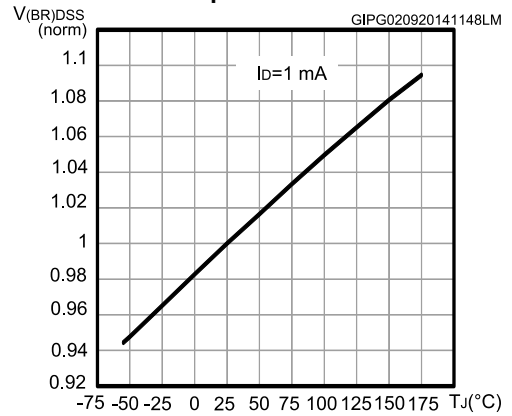
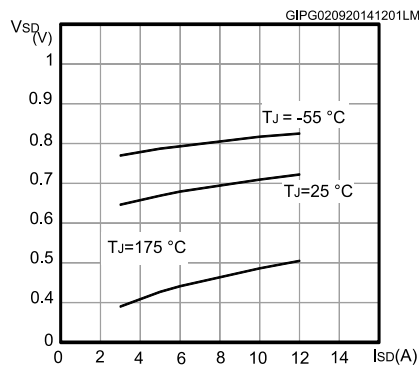
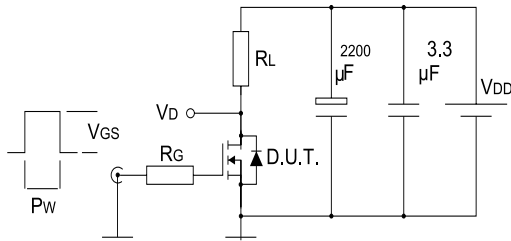


Figure 12: Source-drain diode forward characteristics



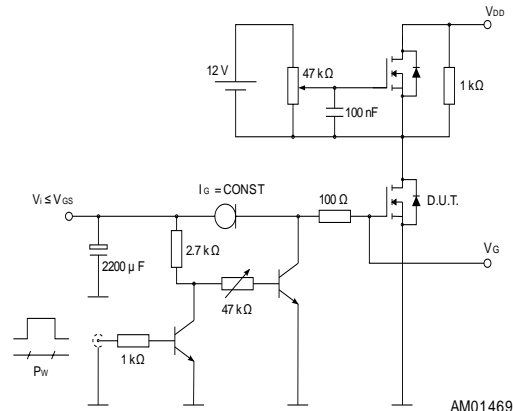
4 Test circuits

Figure 13: Switching times test circuit for resistive load



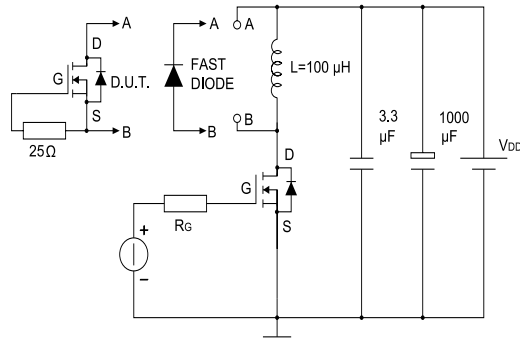
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Figure 14: Gate charge test circuit



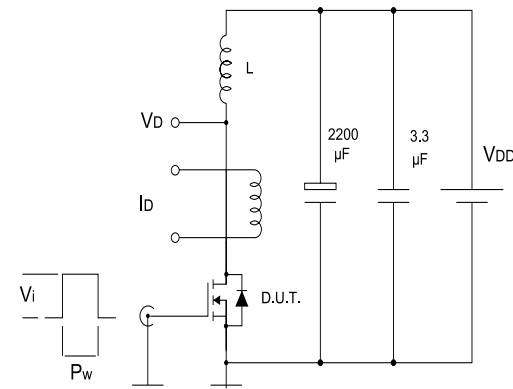
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Figure 15: Test circuit for inductive load switching and diode recovery times



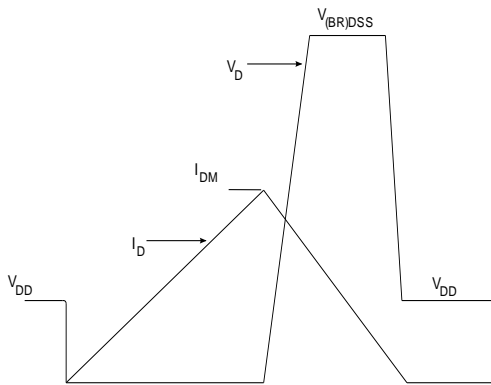
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Figure 16: Unclamped inductive load test circuit



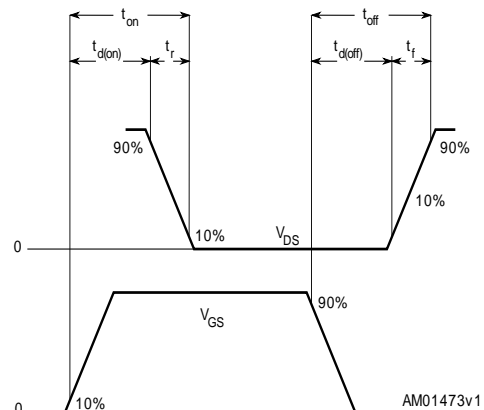
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 SO-8 package mechanical data

Figure 19: SO-8 drawings

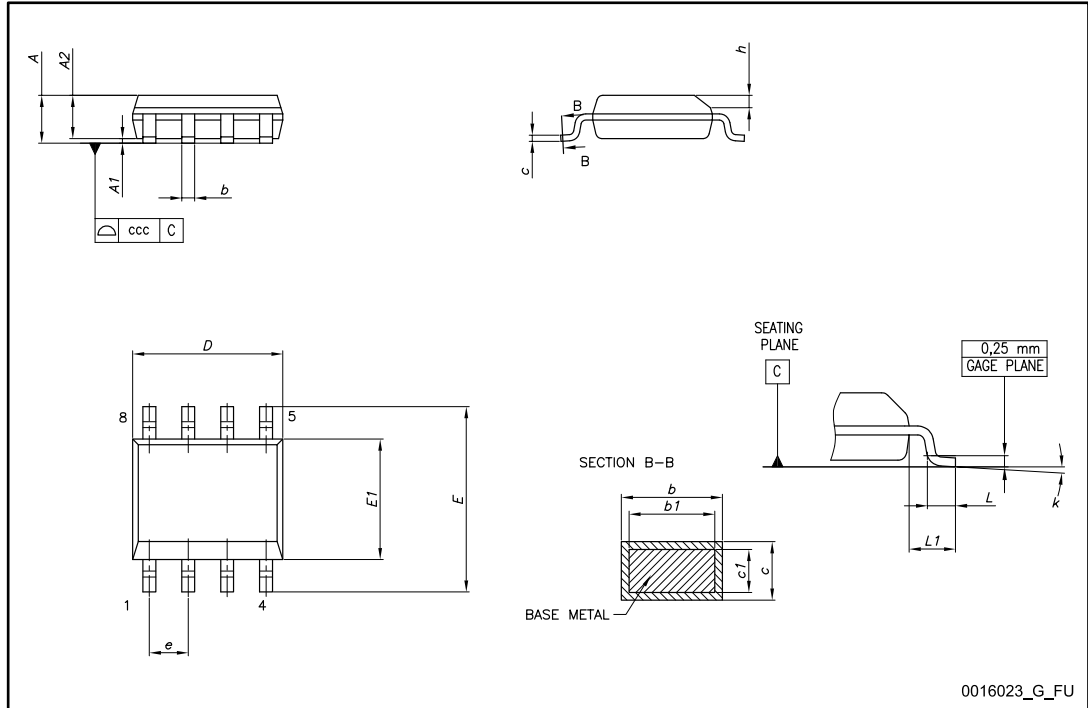
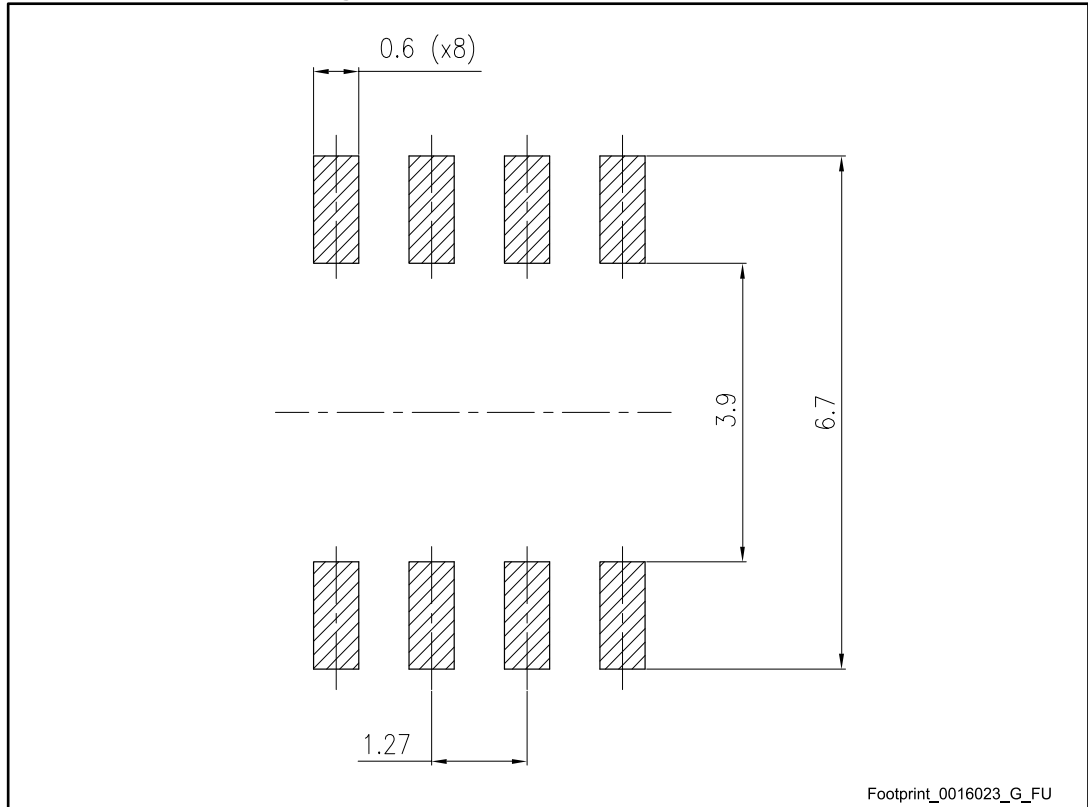


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 20: SO-8 recommended footprint



All dimensions are in mm

6 Packaging mechanical data

Figure 21: SO-8 tape and reel dimensions

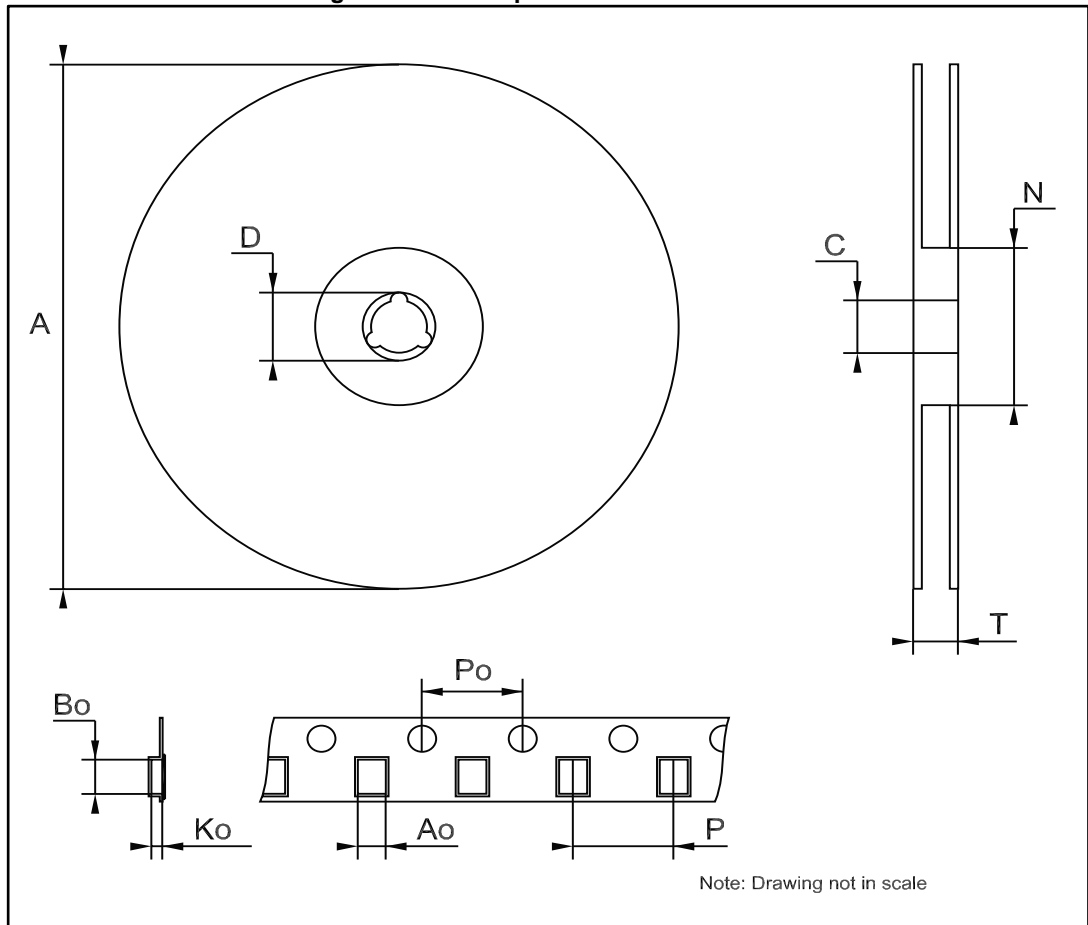


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

7 Revision history

Table 10: Revision history

Date	Revision	Changes
20-Jan-2014	1	First revision.
09-Sep-2014	2	Changed the title. Updated <i>Section "Features"</i> and <i>Section "Description"</i> . Updated <i>Table 4: "On/off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> , <i>Table 7: "Source-drain diode"</i> . Added <i>Section 3: "Electrical characteristics (curves)"</i> .
16-Dec-2014	3	Document status promoted from preliminary data to production data. Minor text changes.

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