Ordering number : ENA1277

SANYO Semiconductors
DATA SHEET

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Bi-CMOS LSI

LV5256GP — Operating Mode Switching Type Step-Up/Down Converter

Overview

The LV5256GP is an operating mode switching type step-up/step-down converter that can switch the operating mode by using the external signal.

Functions

- Built-in Pch gate drive power supply
- Output short-circuit detection by monitoring the input side of the error amplifier
- OCP timer function
- Software start function
- Support for tracking function
- Built-in thermal protection circuit
- Built-in UVLO
- ON/OFF function: Off-time input current smaller than 1μA
- Oscillation frequency : 300kHz to 1.5MHz Oscillation frequency can be set by an external resistor

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input voltage	V_{IN} max		12	V
	V_{DD} max		3.6	V
Maximum output voltage	V_O max		16	V
Maximum output current	I_O max	Between OUT and SW	650	mA
Allowable input pin voltage	V_{CONT} max	RT, FB, IN, OCP, SS, ONOFF, TRAC_IN, DU_SEL, OPC_SEL pins	V_{DD}	V
Allowable power dissipation	Pd max	Mounted on a specified board *	0.8	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

* Specified board : 50mm × 40mm × 0.8mm, glass epoxy 4-layer circuit board (2S2P).

Recommended Operating Conditions at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Input voltage range		V_{IN}		4.5 to 10	V
		V_{DD}		2.9 to 3.1	V
Output voltage range	Step-down	V1	When in normal operation mode	1.0 to V_{IN}	V
		V2	When in tracking operation mode	0 to V_{IN}	V
	Step-up	$V_{OUT}1$	When in normal operation mode	5.3 to 14	V
		$V_{OUT}2$	When in tracking operation mode	V_{IN} to	V
Output current		IO		600	mA

Electrical Characteristics at Ta = 25°C, V_{DD} = 3.0V, V_{IN} = 6.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage						
Reference voltage for comparison	Vref		-1%	1.0	-1%	V
Error amplifier						
Input voltage range	Vrange		0		1.5	V
Open loop voltage gain	Av		60	110		dB
Unity-gain bandwidth	Ft		2	8		MHz
Output source current	IfboL	IN = 2.0V, FB = 1.0V	2			mA
Output sink current	IfboH	IN = 0V, FB = 0V	100			μA
IN pin source current	IiniL	IN = 0V		100	300	nA
FB pin output range	R_fb		0.1			V
TRAC_IN pin source current	ItracL	IN = 0 to Vref		100	300	nA
TRAC_IN pin input operation range	R_trac		0.1		Vref-0.1	V
Logic input pin block 1 (ONOFF)						
Input voltage H level	VoniH		2.8			V
Input voltage L level	VoniL				0.5	V
Input current H level	IoniH	ONOFF = 3.3V		0		μA
Input current L level	IoniL	ONOFF = 0V		0		μA
Logic input pin block 2 (DU_SEL)						
Input voltage H level	VduiH		2.8			V
Input voltage L level	VduiL				0.5	V
Input pull-down resistance	Rdu			200		kΩ
Logic input pin block 3 (OCP_SEL)						
Input voltage H level	VocpiH		2.8			V
Input voltage L level	VocpiL				0.5	V
Input pull-down resistance	Rocp			100		kΩ
Soft start						
Soft start source current	IssH	SS = 0V	7	10	13	μA
Soft start sink current	IssL	When reset, SS = 1.0V		1		mA
Short-circuit protection, SCP						
Short-circuit protection detection voltage 1	Vsc1	OCP_SEL=GND/OPEN *1		× 0.8		V
Short-circuit protection detection voltage 2	Vsc2	OCP_SEL=REG_0 *1		× 0.4		V
SCP comparator offset voltage	SCPosf	TRAC_IN = 0.7V, operation starts from 0.9V.	-40		40	mV
OCP pin source current	IocpH	When in short-circuit protection detection mode		10		μA
OCP pin sink current	IocpL	When in normal operation mode, OCP = 1.0V	0.3	1	3	mA
OCP timer latch voltage	Vocp		1.1	1.2	1.3	V

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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Therml protection, UVLO							
Thermal protection operating temperature		Tot	Design guarantee value *2		175		°C
Thermal protection hysteresis		Dot	Design guarantee value *2		20		°C
UVLO lock release voltage 1		VuvloH	REG_O monitored		2.8		V
UVLO lock voltage 1		VuvloL	REG_O monitored		2.5		V
UVLO lock release voltage 2		VuvloH2	V_{IN} pin voltage		3.8		V
UVLO lock voltage 2		VuvloL2	V_{IN} pin voltage		3.5		V
Oscillator							
Oscillation frequency		F	RT = 100kΩ	0.8	1	1.2	MHz
Oscillation frequency range		R_F		0.3		1.5	MHz
Triangular wave lower-side threshold value		VtriL	RT = 100kΩ		0.5		V
Triangular wave upper-side threshold value		VtriH	RT = 100kΩ		1.0		V
Power supply pin block							
Current drain		Ivin1	V_{IN} pin, when converter is in 1MHz operation mode.		2	4	mA
		Ivin2	V_{IN} pin, when in ONOFF stop mode.			1.0	μA
		Ivdd1	V_{DD} pin, when in ONOFF stop mode.			1.0	μA
Vout-5V Regulator							
Output voltage		Voutm5	Vout-5V regulator, VOUT = 10.0V	VOUT-4.5	VOUT-5	VOUT-5.5	V
Drooping current		Ivoutm5	Vout-5V regulator		20		mA
Internal 3.3V Regulator							
Output voltage		Vreg_o	Ireg_o = 2.0mA	3.0	3.3	3.6	V
Drooping current		Ireg_o	Vreg_o = 2V, V_{IN} = 5V		10		mA
Output characteristics							
Main switch on resistance (Pch)		RonH	V_{IN} = 5V		0.7		Ω
Main switch on resistance (Nch)		RonL	V_{IN} = 5V		0.7		Ω
Through current prevention dead time		Tdead			25		ns
Maximum on-duty (step-down)		DMAX1	RT = 100kΩ		100		%
Maximum on-duty (step-up)		DMAX2	RT = 100kΩ		85		%
Converter characteristics							
Efficiency	Step-down	η1	V_{IN} = 5.0V, V = 4.6V, I_O = 200mA		93		%
	Step-up	η2	V_{IN} = 5.0V, VOUT1 = 6.6V, I_O = 200mA		93		%
Line regulation	Step-down	$\Delta V1/V_{IN}$	V_{IN} = 4.5 to 8.6V, V1 = 4.6V, I_O = 200mA	0			%
	Step-up	$\Delta VOUT1/V_{IN}$	V_{IN} = 4.5 to 5.5V, VOUT1 = 6.6V, I_O = 200mA	0			%
Load regulation	Step-down	$\Delta V1/I_O$	V_{IN} = 8.4V, V1 = 4.6V, I_O = 0 to 200mA	0			
	Step-up	$\Delta VOUT1/I_O$	V_{IN} = 5.0, VOUT1 = 6.6V, I_O = 200mA	0			

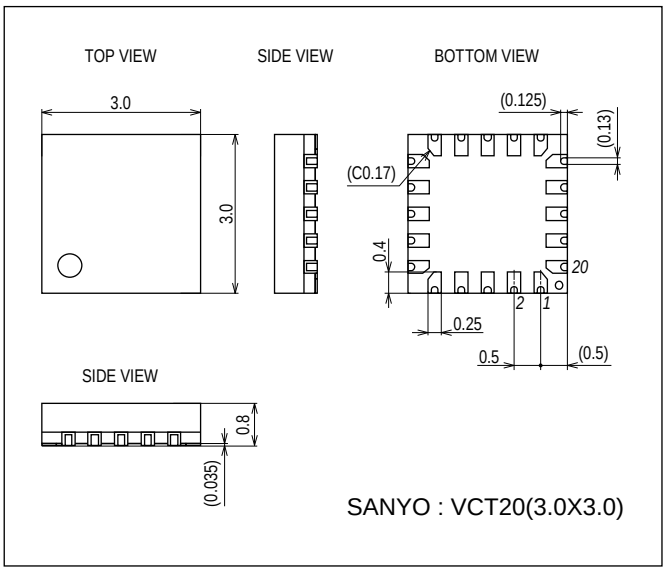
*1 IN pin voltage is the detection point. The lowest voltage among Vref, TRAC_IN, and SS is used.

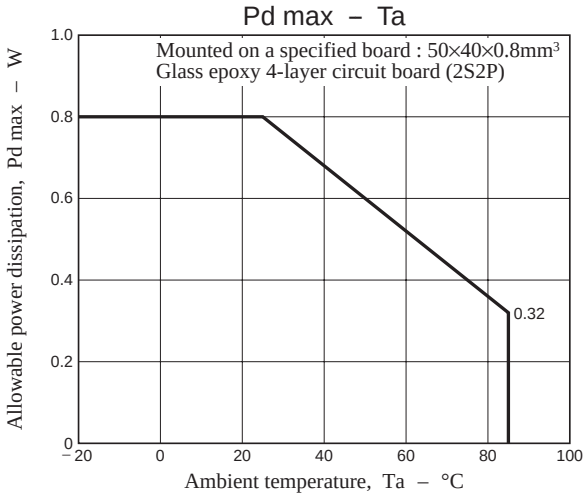
*2 Design guarantee value, and no measurement is performed.

Package Dimensions

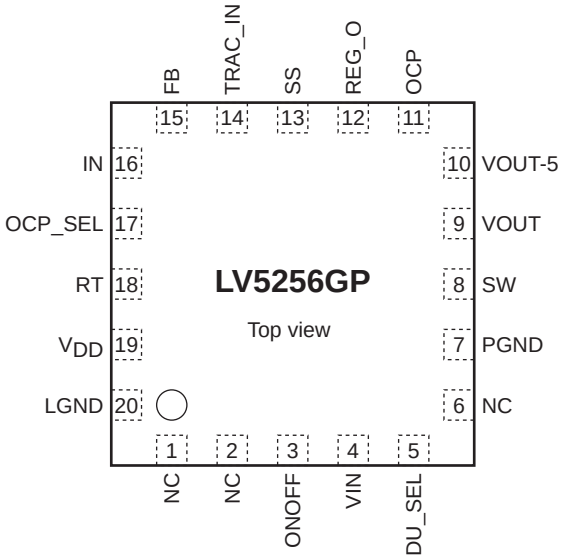
unit : mm (typ)

3368

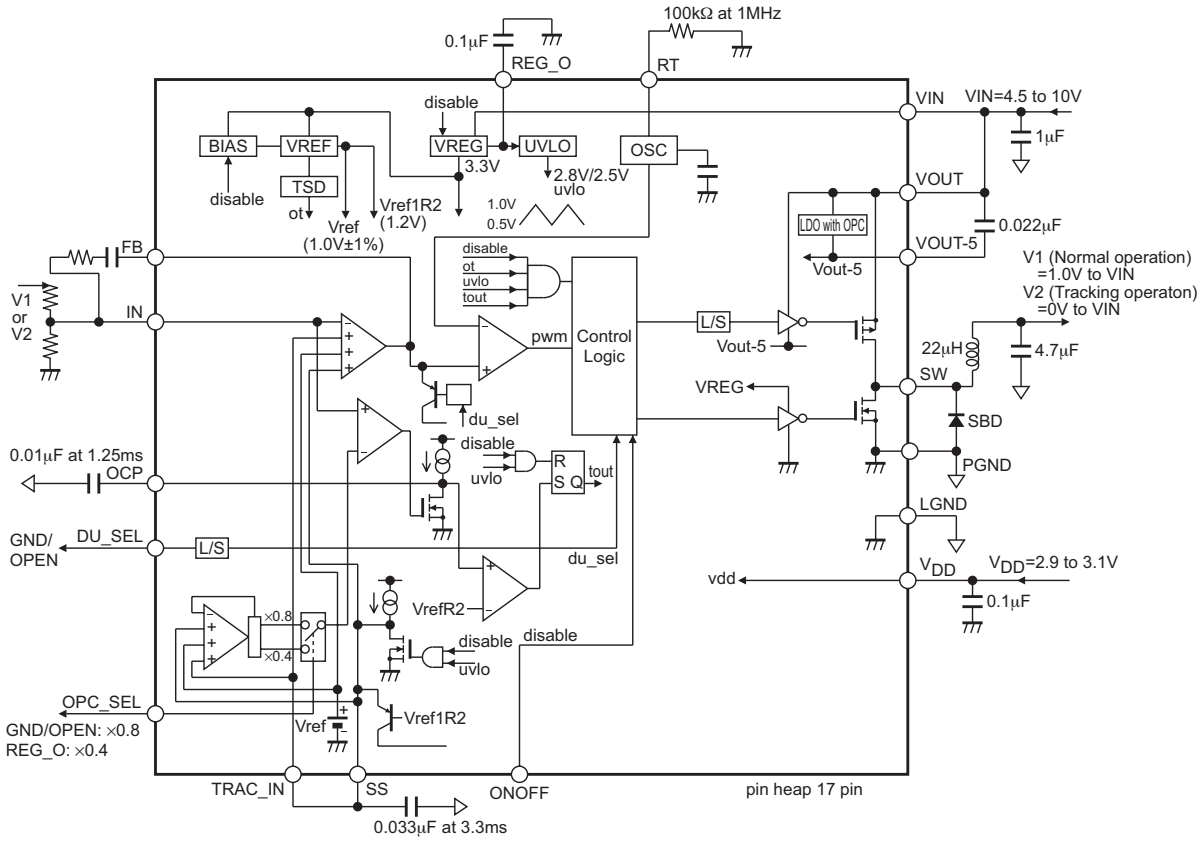




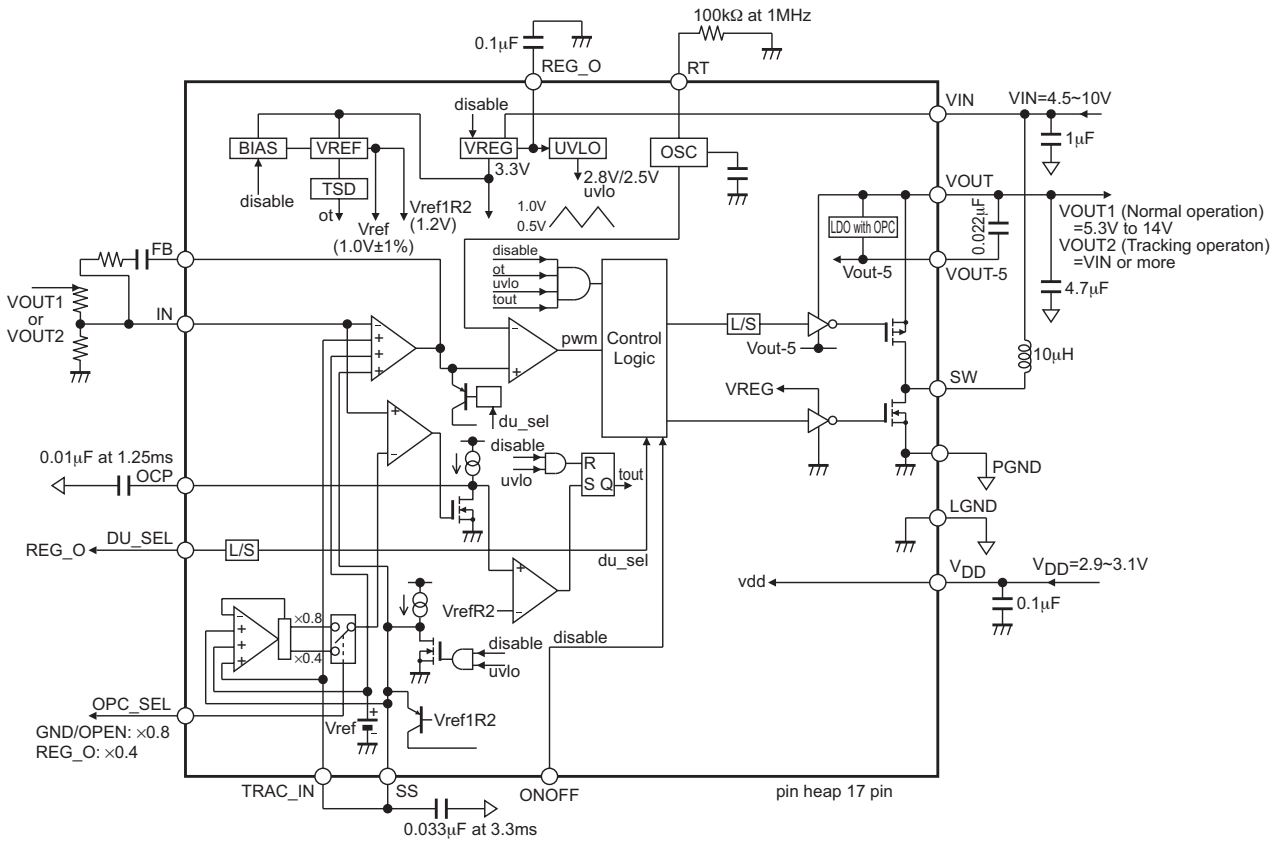
Pin Assignment



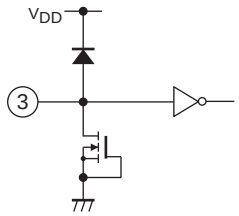
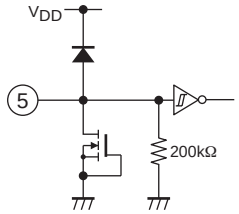
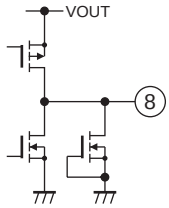
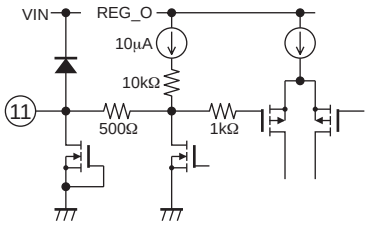
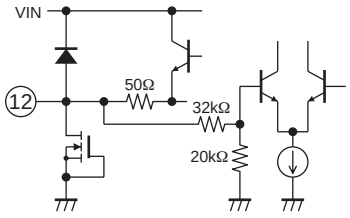
Block Diagrams and Sample Application Circuit 1 (Step-down)



Sample Application Circuit 2 (Step-up)



Pin Functions

Pin No.	Pin Name	Description	Equivalent Circuit
1 2 6	NC	No connection. Must be kept open.	
3	ONOFF	ON/OFF signal input pin. Threshold level is TTL level. Maximum withstand voltage is V_{DD}.	
4	VIN	Power supply pin of the IC. Apply the input voltage.	
5	DU_SLE	Step-up/down switching pin. The IC goes in step-up mode by connecting this pin to REG_O pin, and in step-down mode by connecting this pin to GND or leaving this pin open. An internal pull-down resistor (200kΩ) is provided between DU_SEL and GND pins.	
7	PGND	Power ground pin. The source of the output transistor (Nch-MOSFET) is connected.	
8	SW	Switching element. A 0.7Ω (typ) Nch switch is inserted between this pin and PGND, and a 0.7Ω (typ) Pch switch is connected between this pin and VOUT. In step-down mode, insert an inductor between the switching node and power supply output, and in step-up mode insert an inductor between this pin and power supply input.	
9	VOUT	Source potential of the internal Pch-MOSFET. In step-down mode, apply the input voltage. In step-up mode, apply the power supply voltage.	
10	VOUT-5	Internal Pch-MOSFET gate suplly voltage generation pin. Used to generate a voltage with a level equal to VOUT pin voltage-5V by the internal LDO with OCP.	
11	OCP	Overcurrent detection timer setup pin. Connect a capacitor between this pin and ground to define the time interval between the beginning of the overcurrent state and the IC latches off. The capacitor is charged by the 10μA internal constant current source. If the OCP_SEL pin is kept open or connected to GND, the IC identifies a short-circuit and starts the timer counter when the voltage at the IN pin falls below 0.8 times the voltage of Vref, TRAC_IN or SS, whichever is lower. If the OCP_SEL pin is connected to REG_O, the IC compares the voltage at the IN pin with 0.4 times the voltage. When the voltage at this pin goes beyond 1.25V, the IC latches off. The latch-off state is reset by the off signal at the ON/OFF pin or the UVLO lock.	
12	REG_O	3.3V regulator output pin.	

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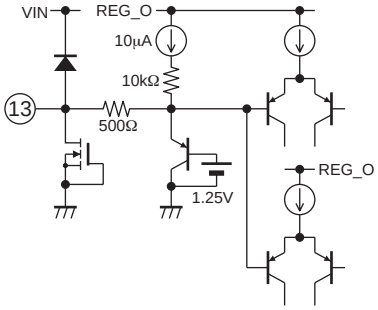
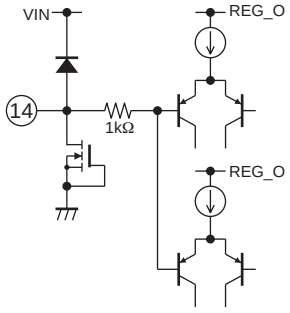
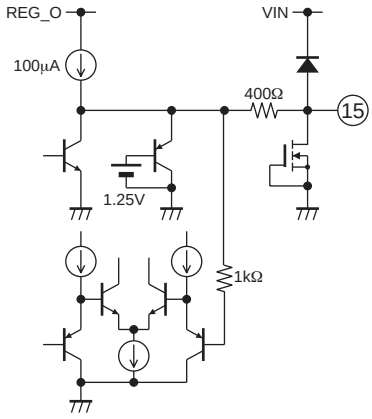
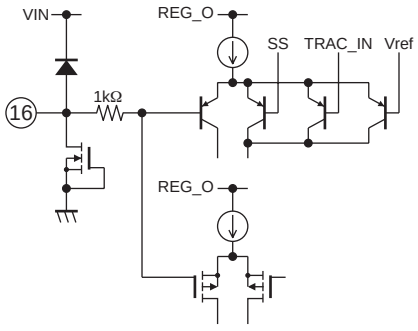
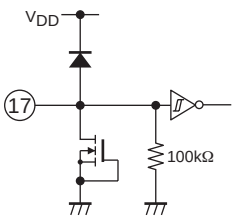
Pin No.	Pin Name	Description	Equivalent Circuit
13	SS	Capacitor connection pin for soft start. The capacitor connected to this pin is charged by the internal 10μA constant current. The interval during which this voltage reaches Vref is called the soft start period. The voltage is clipped to approx. 2V after the soft start. This pin is pulled down to the ground level when ONOFF/UVLO lock mode.	
14	TRAC_IN	Reference voltage input pin for tracking power supply operating. A voltage from 0V up to Vref applied to this pin serves as the reference voltage for determining the output voltage. This pin must be connected to the SS pin when it is not to be used.	
15	FB	Error amplifier output pin. Connect a phase compensation component between this pin and IN pin.	
16	IN	Output voltage input pin. Apply the resistor divided output voltage to this pin.	
17	OCP_SEL	OCP detection voltage switching pin, A 100kΩ pull-down resistor is provided between OCP_SEL and GND. The IC enters the 0.8 times detection mode when this pin is connected to GND or kept open and enters the 0.4 times detection mode when the pin is connected to the REG_O pin.	

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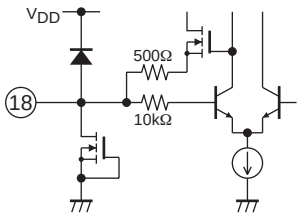
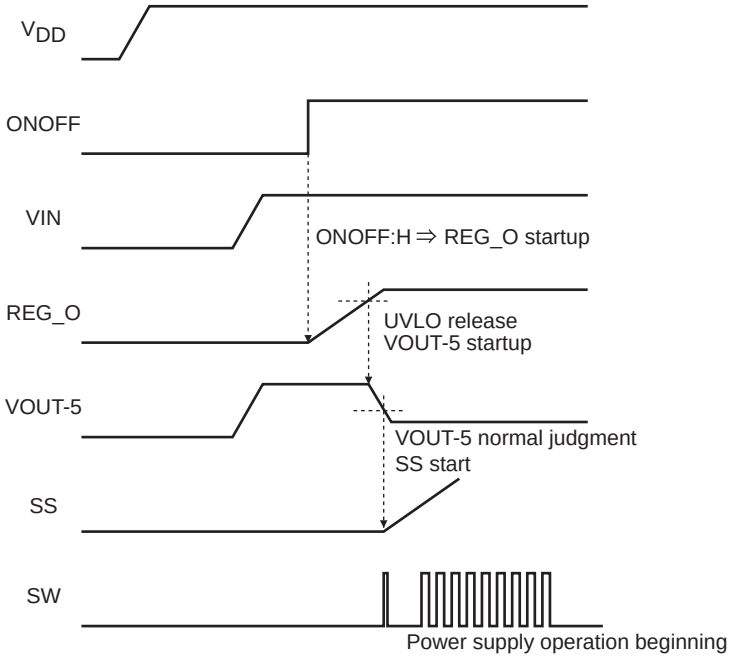
Pin No.	Pin Name	Description	Equivalent Circuit
18	RT	Oscillation frequency setting pin. Connect a resistor between this pin and GND. A 100kΩ resistor causes the oscillator to oscillate at 1MHz (typ.).	
19	V_{DD}	Logic system power supply. Apply 3.0V±0.1V to this pin from an external source.	
20	LGND	Logic system ground pin. All voltages are measured with respect to this voltage level.	

Startup Sequence

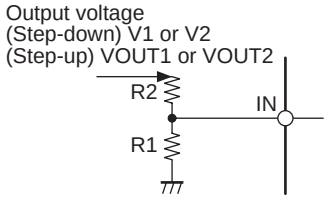


***** Be sure to set the ONOFF to 0V when starts or stops V_{DD}. And apply voltage to VIN after V_{DD} started up.

Output Voltage Setting Method

The LV5256GP can produce any arbitrary output voltage. The output voltage is set by the resistor inserted between the IN pin (pin 16) and GND, and IN pin and output voltage.

The calculating formula for setting the output voltage by using the output voltage setup lower-side resistor R1 and the output voltage setup upper-side resistor R2 is as follows:



$$(Output\ voltage) = \left(1 + \frac{R2}{R1}\right) \times Vref = 1 + \frac{R2}{R1} \quad \because Vref = 1.00\,(typ)$$