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FQD4P25TM_WS

P-Channel QFET® MOSFET

-250 V, -3.1 A, 2.1 Ω

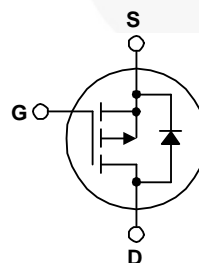
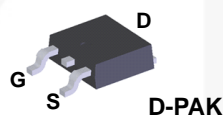


Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -3.1 A, -250 V, $R_{DS(on)} = 2.1 \Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = -1.55 \text{ A}$
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 10.3 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQD4P25TM_WS	Unit
V_{DSS}	Drain-Source Voltage	-250	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	-3.1	A
	- Continuous ($T_C = 100^\circ\text{C}$)	-1.96	A
I_{DM}	Drain Current - Pulsed (Note 1)	-12.4	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	280	mJ
I_{AR}	Avalanche Current (Note 1)	-3.1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	45	W
	- Derate above 25°C	0.36	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FQD4P25TM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD4P25TM_WS	FQD4P25S	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	--	-0.21	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -250\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -200\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.55\text{ A}$	--	1.63	2.1	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -1.55\text{ A}$	--	2.0	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	325	420	pF
C_{oss}	Output Capacitance		--	65	85	pF
C_{rss}	Reverse Transfer Capacitance		--	10	13	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -125\text{ V}, I_D = -4.0\text{ A},$ $R_G = 25\ \Omega$	--	9.5	30	ns	
t_r	Turn-On Rise Time		--	60	130	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	14	40	ns
t_f	Turn-Off Fall Time		(Note 4)	--	27	65	ns
Q_g	Total Gate Charge	$V_{DS} = -200\text{ V}, I_D = -4.0\text{ A},$ $V_{GS} = -10\text{ V}$	--	10.3	14	nC	
Q_{gs}	Gate-Source Charge		(Note 4)	--	2.7	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	5.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-3.1	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-12.4	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.1\text{ A}$	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -4.0\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	140	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.64	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum Junction temperature.
2. $L = 46.6\text{ mH}, I_{AS} = -3.1\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -4.0\text{ A}, di_V/dt \leq 300\text{ AV}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

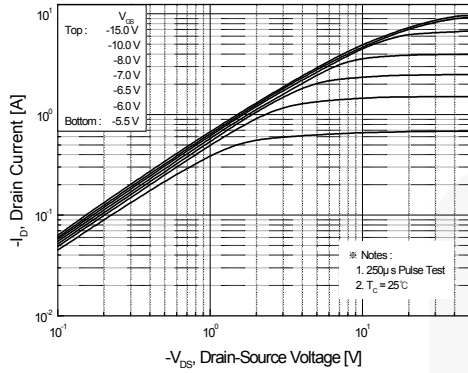


Figure 1. On-Region Characteristics

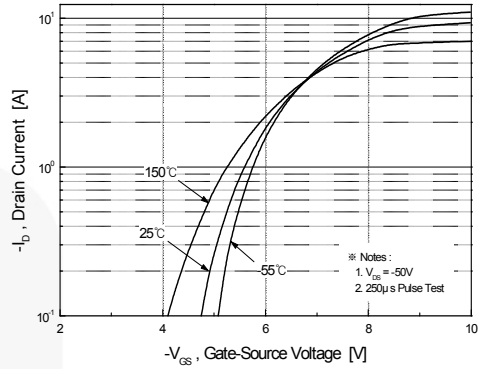


Figure 2. Transfer Characteristics

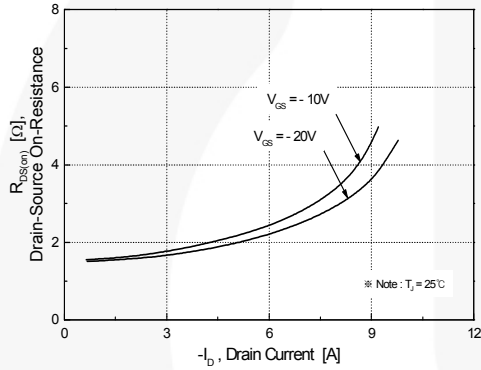


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

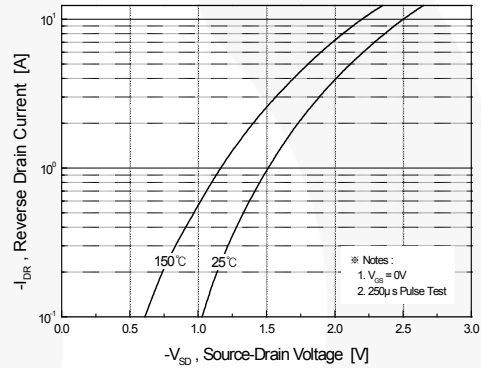


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

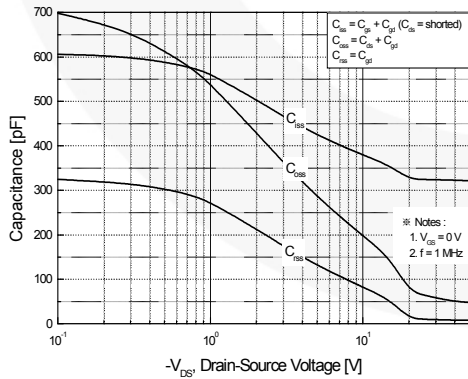


Figure 5. Capacitance Characteristics

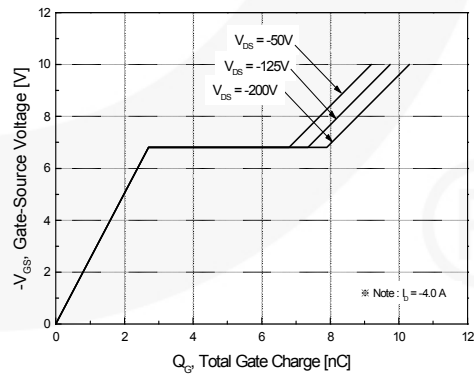


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

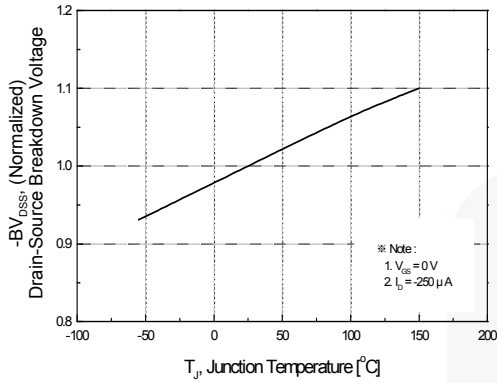


Figure 7. Breakdown Voltage Variation vs. Temperature

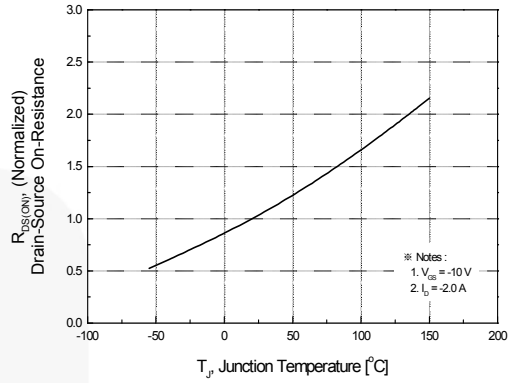


Figure 8. On-Resistance Variation vs. Temperature

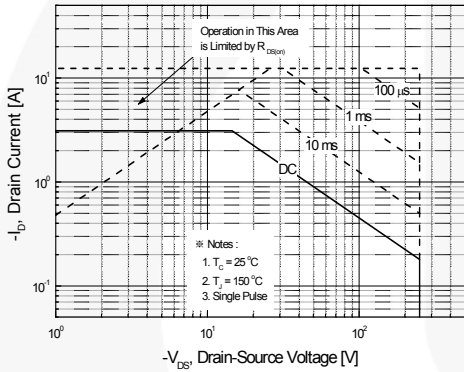


Figure 9. Maximum Safe Operating Area

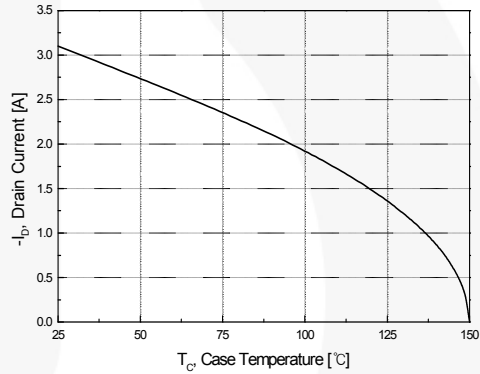


Figure 10. Maximum Drain Current vs. Case Temperature

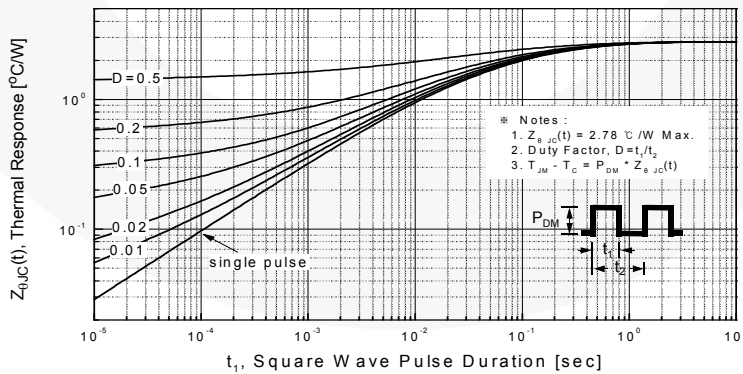


Figure 11. Transient Thermal Response Curve

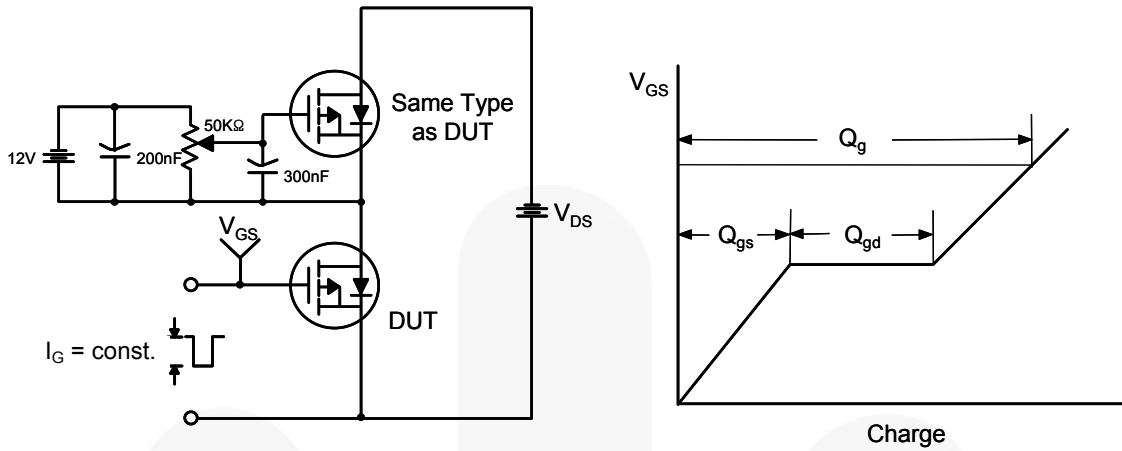


Figure 12. Gate Charge Test Circuit & Waveform

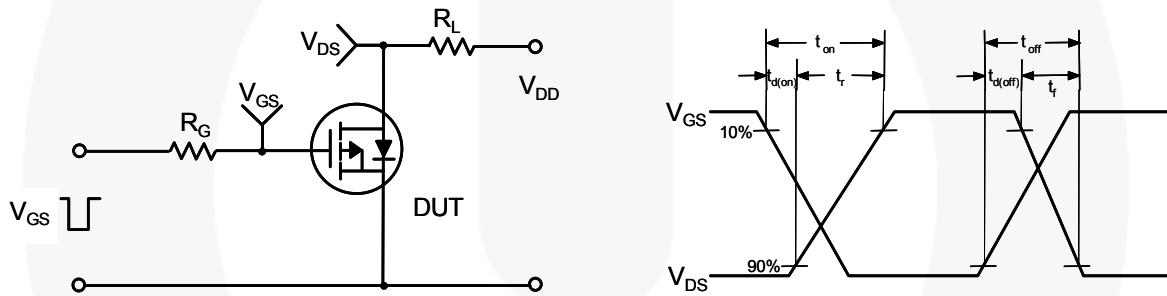


Figure 13. Resistive Switching Test Circuit & Waveforms

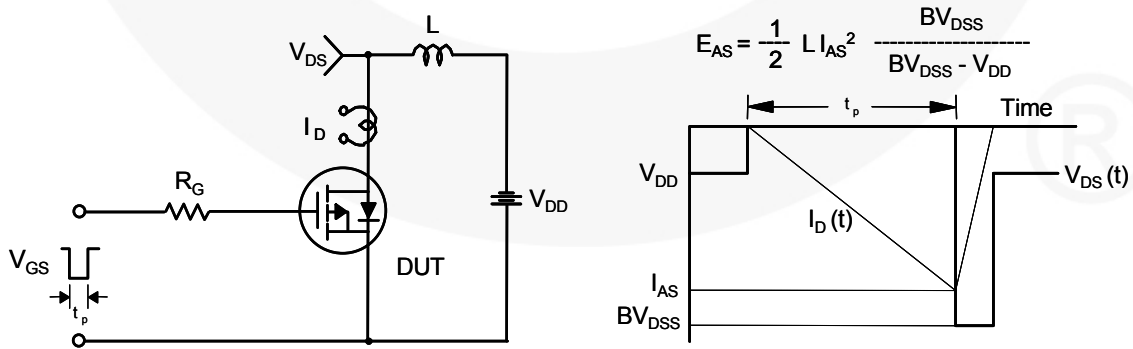


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

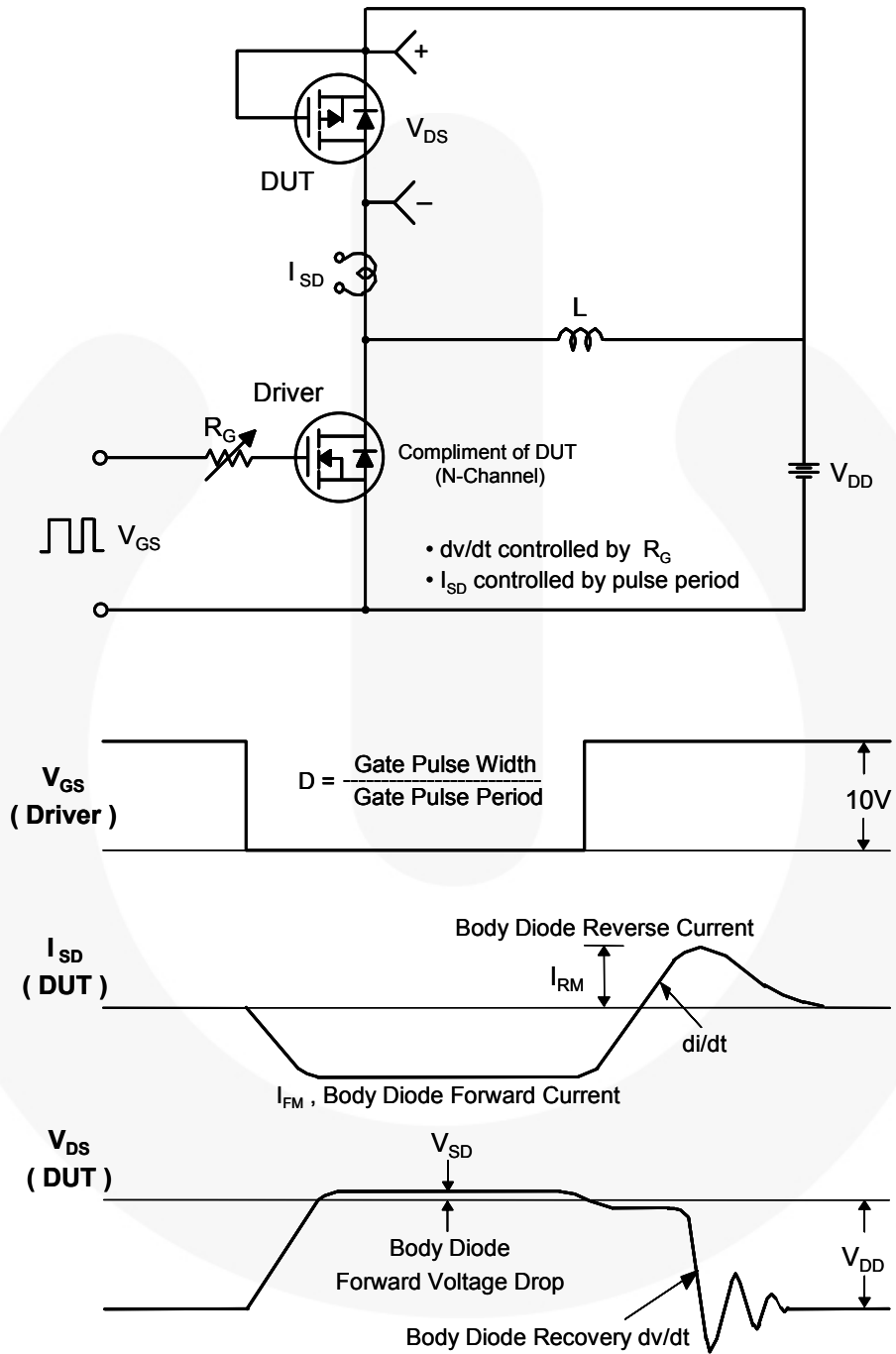


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

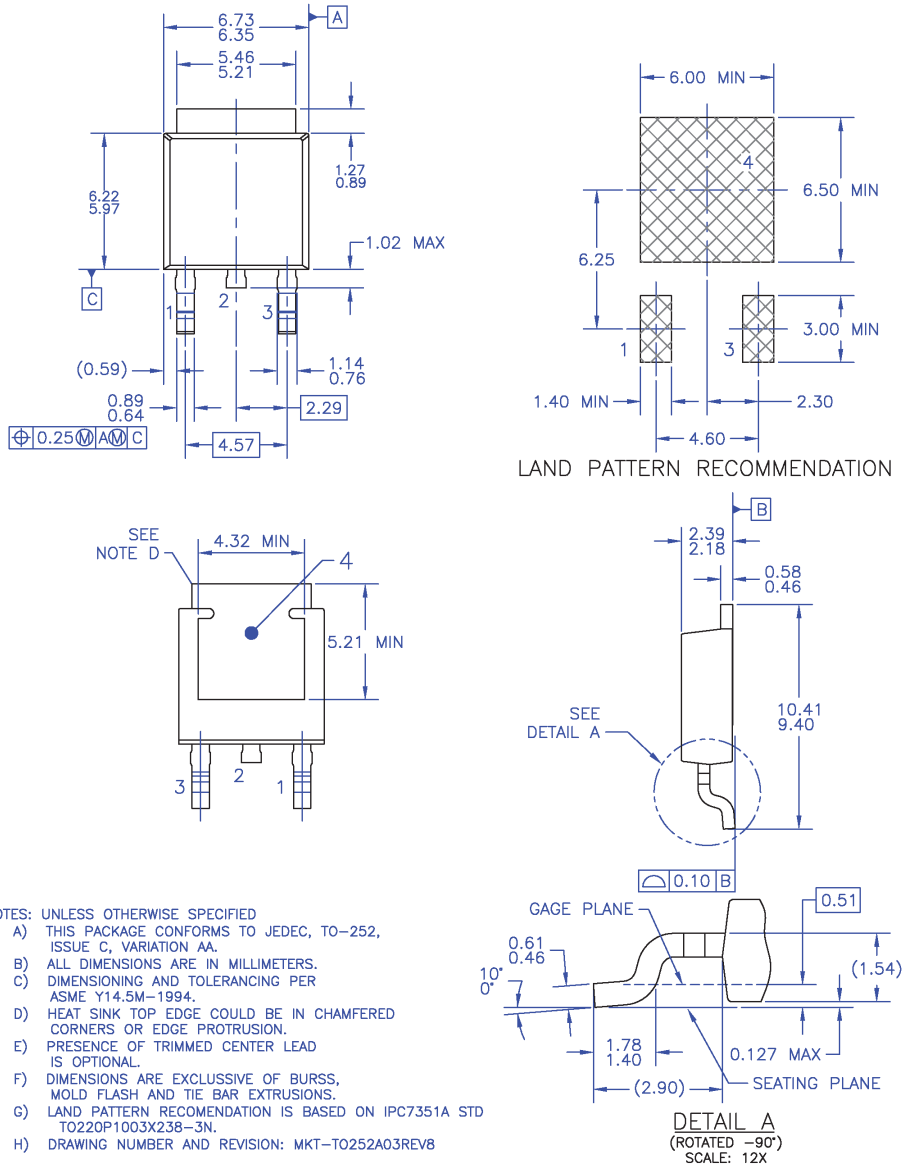


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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