Freescale Semiconductor
Technical Data

Document Number: MRF8S21200H
Rev. 2, 10/2010

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF8S21200HR6
MRF8S21200HSR6

2110-2170 MHz, 48 W AVG., 28 V
W-CDMA, LTE
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for W-CDMA and LTE base station applications with frequencies from 2110 to 2170 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

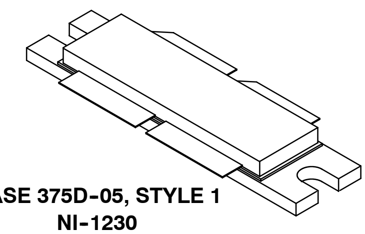
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1400 mA, P_{out} = 48 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	17.8	32.6	6.4	-37.7
2140 MHz	18.1	32.6	6.3	-37.1
2170 MHz	18.1	32.9	6.2	-36.2

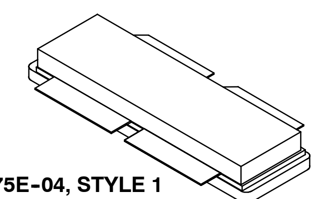
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 250 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.



CASE 375D-05, STYLE 1
NI-1230
MRF8S21200HR6



CASE 375E-04, STYLE 1
NI-1230S
MRF8S21200HSR6

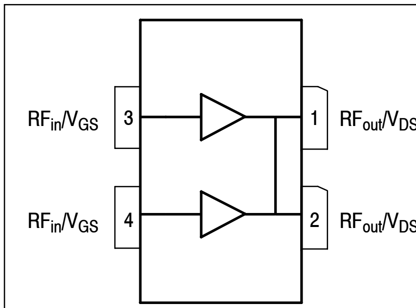


Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
CW Operation @ T_A = 25°C Derate above 25°C	CW	200 1.6	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 48 W CW, 28 Vdc, I_{DQ} = 1400 mA Case Temperature 81°C, 200 W CW, 28 Vdc, I_{DQ} = 1400 mA	$R_{\theta JC}$	 0.31 0.27	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1400 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.7	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	0.1	0.17	0.3	Vdc

Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 48 W Avg., f = 2140 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	16.5	18.1	19.5	dB
Drain Efficiency	η_D	30.0	32.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.1	-35.0	dBc
Input Return Loss	IRL	—	-15	-7	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 48 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

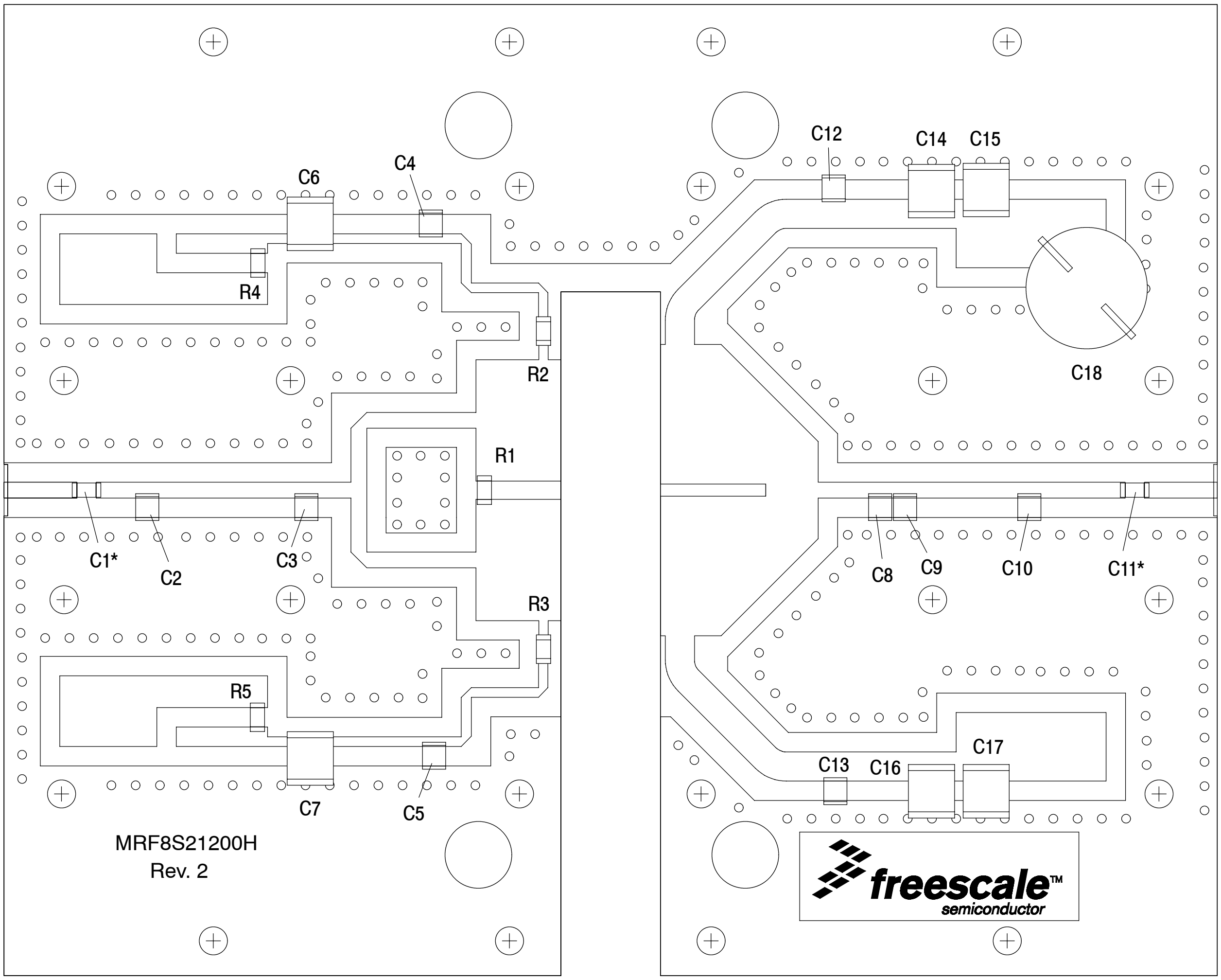
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	17.8	32.6	6.4	-37.7	-15
2140 MHz	18.1	32.6	6.3	-37.1	-15
2170 MHz	18.1	32.9	6.2	-36.2	-13

1. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 2110-2170 MHz Bandwidth					
IMD Symmetry @ 140 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	8	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	35	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 48 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.02	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.02	—	dB/°C



*C1 and C11 are mounted vertically.

Figure 2. MRF8S21200HR6(HSR6) Test Circuit Component Layout

Table 5. MRF8S21200HR6(HSR6) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C5, C11, C12, C13	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C2	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C3	0.6 pF Chip Capacitor	ATC100B0R6BT500XT	ATC
C6, C7, C14, C15, C16, C17	10 μF, 50 V Chip Capacitors	C5750X5R1H106MT	TDK
C8	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C9	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C10	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C18	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	22 Ω, 1/4 W Chip Resistor	CRCW120622R0FKEA	Vishay
R2, R3	12 Ω, 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
R4, R5	0 Ω, 3 A Chip Resistors	CRCW12060000Z0EA	Vishay
PCB	0.030″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS

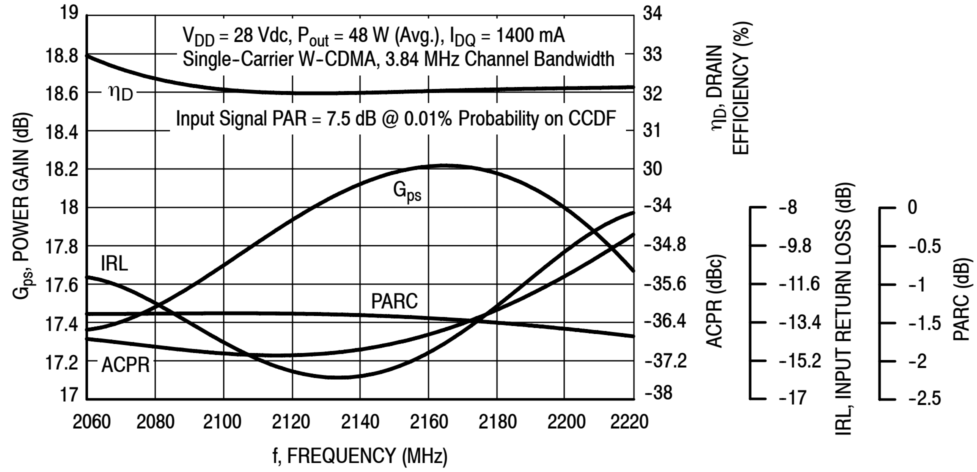


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 48 Watts Avg.

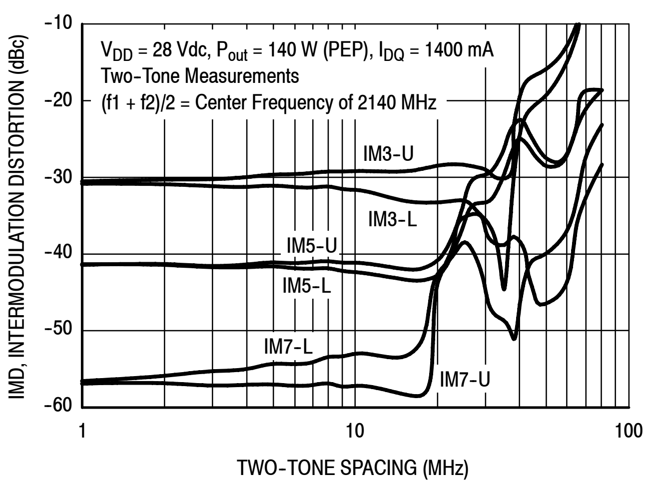


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

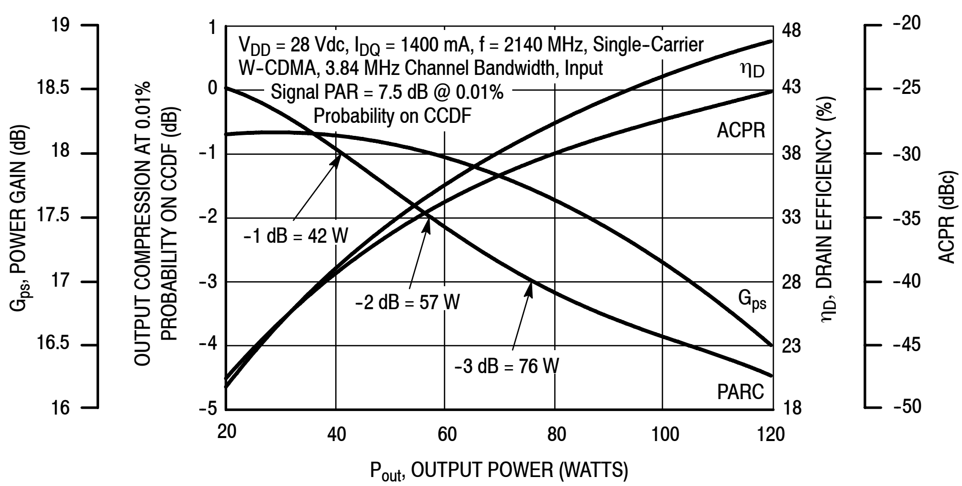


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

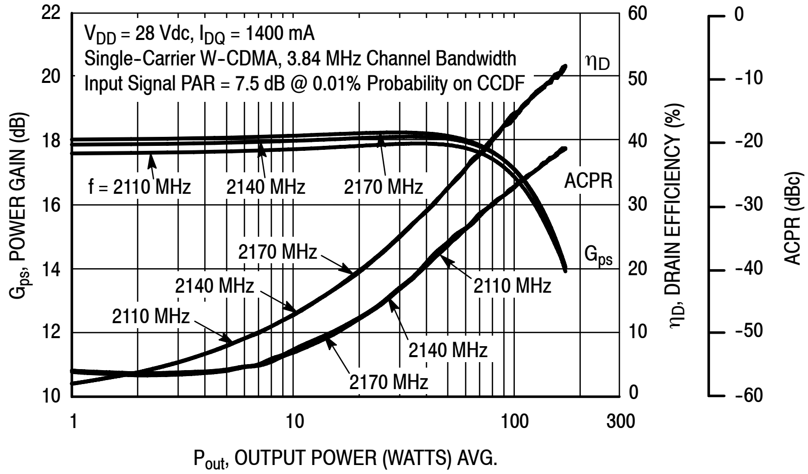


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

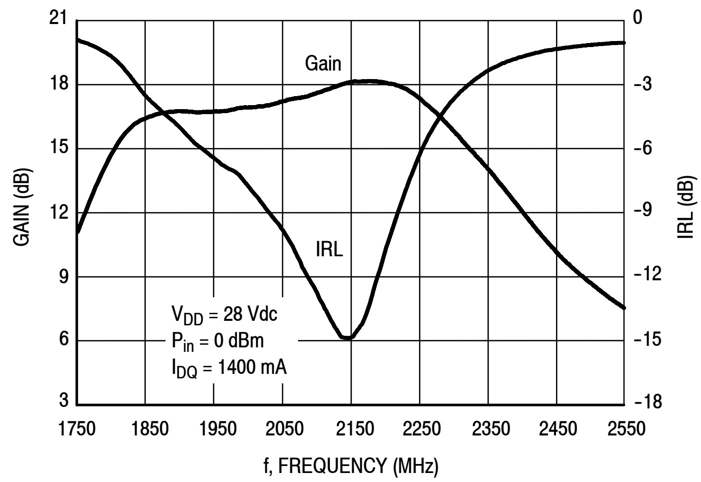


Figure 7. Broadband Frequency Response

W-CDMA TEST SIGNAL

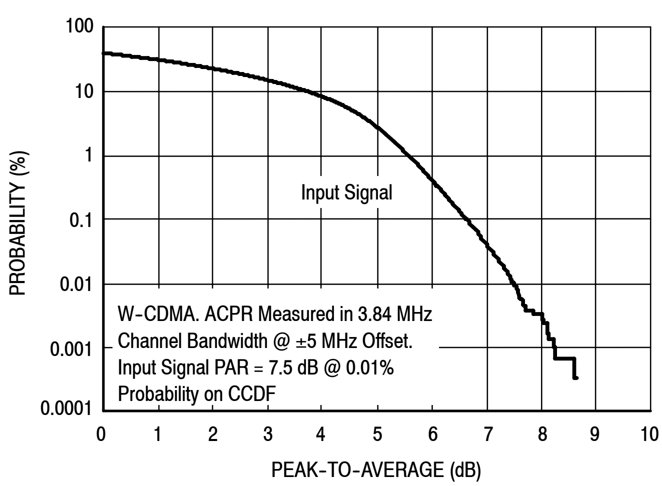


Figure 8. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

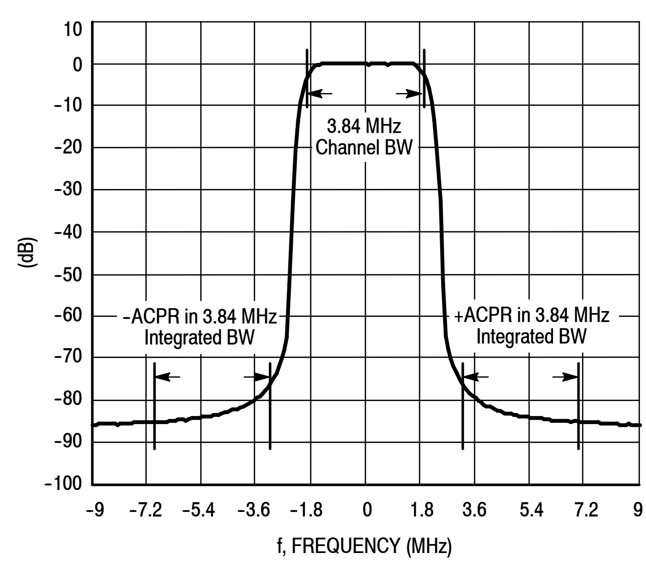


Figure 9. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 48 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	3.64 - j4.51	1.42 - j2.27
2080	3.65 - j4.50	1.41 - j2.21
2100	3.64 - j4.53	1.40 - j2.15
2120	3.56 - j4.47	1.40 - j2.09
2140	3.58 - j4.44	1.39 - j2.03
2160	3.58 - j4.44	1.38 - j1.97
2180	3.57 - j4.44	1.38 - j1.91
2200	3.56 - j4.45	1.38 - j1.86
2220	3.54 - j4.64	1.37 - j1.80

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

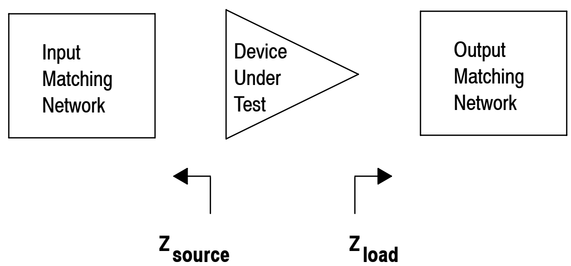
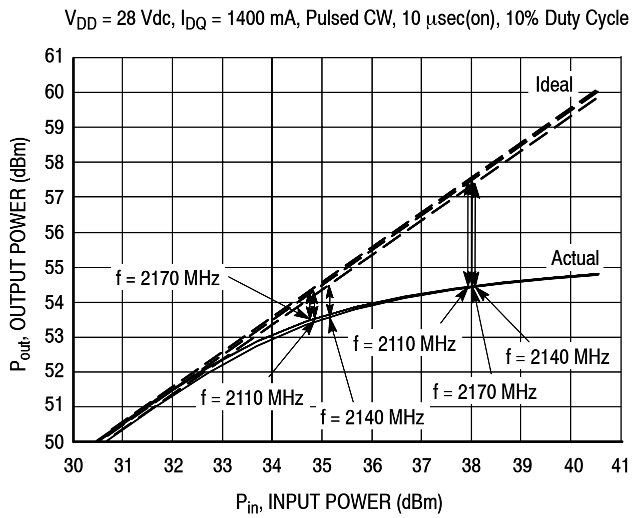


Figure 10. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

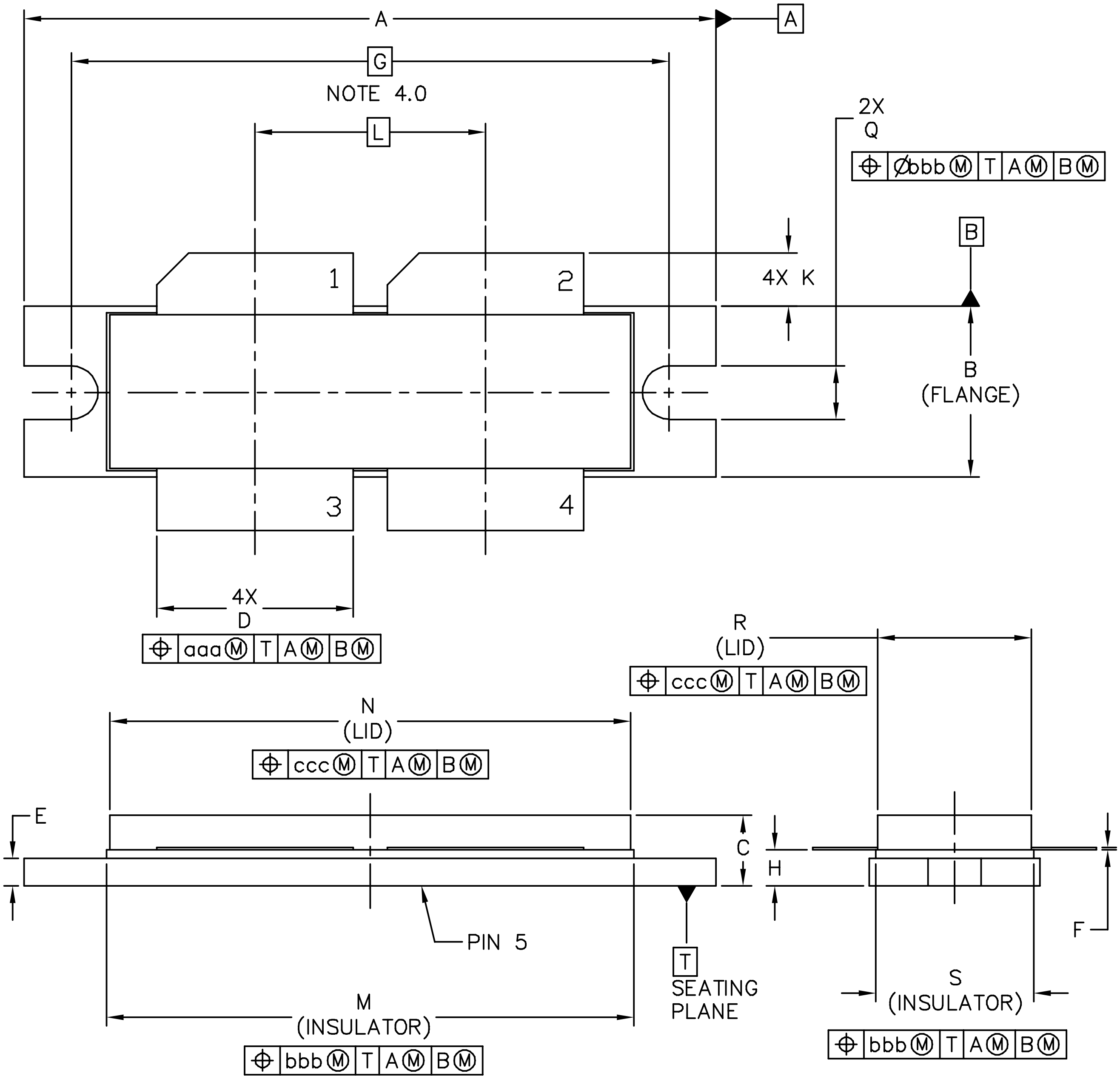
f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2110	231	53.6	276	54.4
2140	230	53.6	279	54.5
2170	229	53.6	277	54.4

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
2110	P1dB	2.14 - j5.14	0.77 - j1.44
2140	P1dB	3.28 - j6.37	0.75 - j1.52
2170	P1dB	5.59 - j7.20	0.67 - j1.41

Figure 11. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS



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	CASE NUMBER: 375D–05	31 MAR 2005	
	STANDARD: NON–JEDEC		

NOTES:

1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

2.0 CONTROLLING DIMENSION: INCH

3.0 DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

4.0 RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

STYLE 1:
PIN 1 - DRAIN
2 - DRAIN
3 - GATE
4 - GATE
5 - SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55
B	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.3
C	.150	.200	3.81	5.08	R	.355	.365	9.01	9.27
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53
E	.062	.066	1.57	1.68					
F	.004	.007	0.1	0.18					
G	1.400 BSC		35.56 BSC		aaa	.013		0.33	
H	.082	.090	2.08	2.29	bbb	.010		0.25	
K	.117	.137	2.97	3.48	ccc	.020		0.51	
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					

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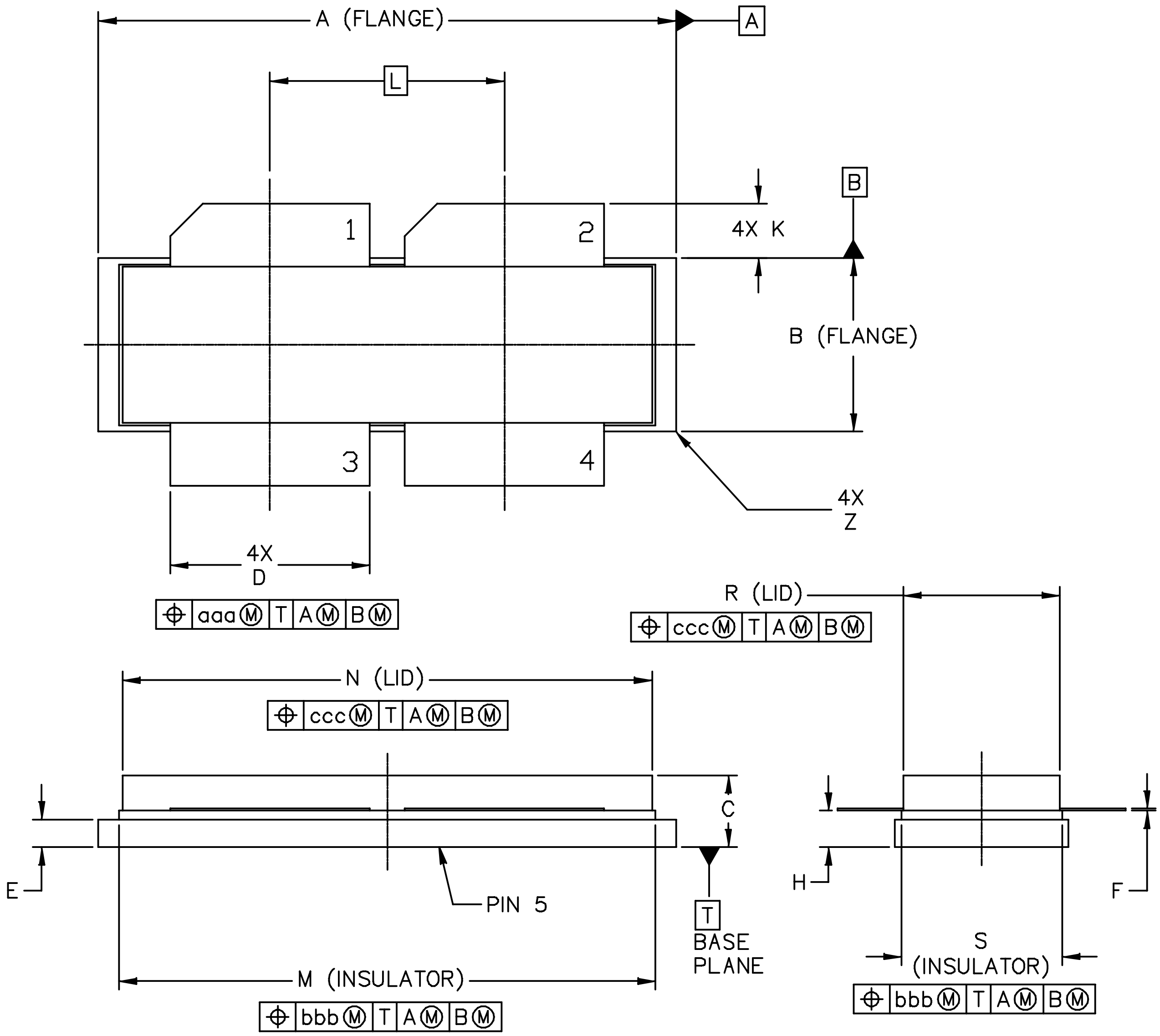

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	CASE NUMBER: 375E–04		05 AUG 2005
	STANDARD: NON–JEDEC		

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION H IS MEASURED .030 AWAY FROM PACKAGE BODY

STYLE 1:
PIN 1 — DRAIN
2 — DRAIN
3 — GATE
4 — GATE
5 — SOURCE

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.265	1.275	32.13	32.38	R	.355	.365	9.01	9.27
B	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
C	.150	.200	3.81	5.08	Z	---	.040	---	1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.1	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

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	CASE NUMBER: 375E-04	05 AUG 2005
	STANDARD: NON-JEDEC	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2009	• Initial Release of Data Sheet
1	Nov. 2009	• Removed Typical P_{out} @ 1 dB Compression Point bullet from p. 1, and P1dB from the Typical Performance table, p. 3. P1dB was artificially low due to fixture tuning tradeoffs, i.e., fixture was tuned for back-off linearity versus optimum P1dB.
2	Oct. 2010	• Changed Human Body Model ESD rating from Class 1A to Class 2 to reflect recent ESD test results of the device, p. 2.

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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
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China
+86 10 5879 8000
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