

PHT2NQ10T

N-channel TrenchMOS transistor

Rev. 01 — 16 October 2001

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

PHT2NQ10T in SOT223

2. Features

- TrenchMOS™ technology
- Fast switching
- Surface mount package.

3. Applications

- Primary side switch in DC to DC converters
- High speed driver
- Fast, general purpose switch.

4. Pinning information

Table 1: Pinning - SOT223, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p style="text-align: center;">SOT223</p>	<p style="text-align: center;"><small>MBB076</small></p>
2	drain (d)		
3	source (s)		
4	drain (d)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25^{\circ}\text{C} \leq t_o \leq 150^{\circ}\text{C}$	–	100	V
I_D	drain current (DC)	$T_{sp} = 25^{\circ}\text{C}; V_{GS} = 10\text{ V}$	–	2.5	A
P_{tot}	total power dissipation	$T_{sp} = 25^{\circ}\text{C}$	–	6.25	W
T_j	junction temperature		–	150	$^{\circ}\text{C}$
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 1.75\text{ A}$	315	430	$\text{m}\Omega$

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

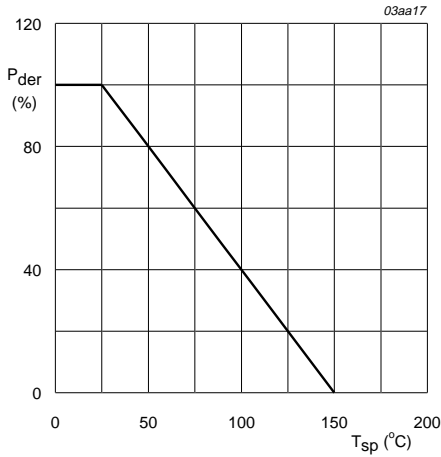
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25^{\circ}\text{C} \leq t_o \leq 150^{\circ}\text{C}$	–	100	V
V_{DGR}	drain-gate voltage (DC)	$25^{\circ}\text{C} \leq t_o \leq 150^{\circ}\text{C}; R_{GS} = 20\text{ k}\Omega$	–	100	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_{sp} = 25^{\circ}\text{C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	–	2.5	A
		$T_{sp} = 100^{\circ}\text{C}; V_{GS} = 10\text{ V};$	–	1.6	A
I_{DM}	peak drain current	$T_{sp} = 25^{\circ}\text{C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	–	10	A
P_{tot}	total power dissipation	$T_{sp} = 25^{\circ}\text{C};$ Figure 1	–	6.25	W
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–65	+150	$^{\circ}\text{C}$

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{sp} = 25^{\circ}\text{C}$	–	2.5	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25^{\circ}\text{C}; t_p \leq 10\text{ }\mu\text{s}$	–	10	A

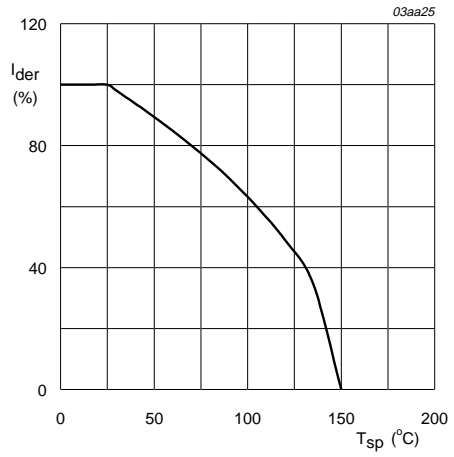
Avalanche ruggedness

E_{AS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 2.5\text{ A};$ $t_p = 0.2\text{ ms}; V_{DD} \leq 15\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting $T_j = 25^{\circ}\text{C};$ Figure 4	–	32	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; $V_{DD} \leq 15\text{ V};$ $R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$ Figure 4	–	2.5	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

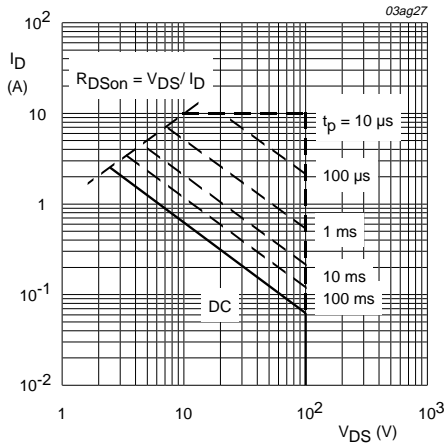
Fig 1. Normalized total power dissipation as a function of solder point temperature.



V_{GS} ≥ 10 V

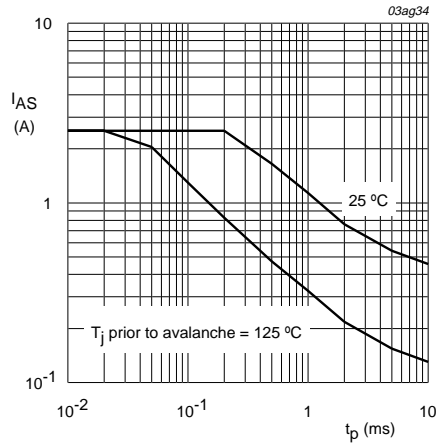
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C and 125 °C.

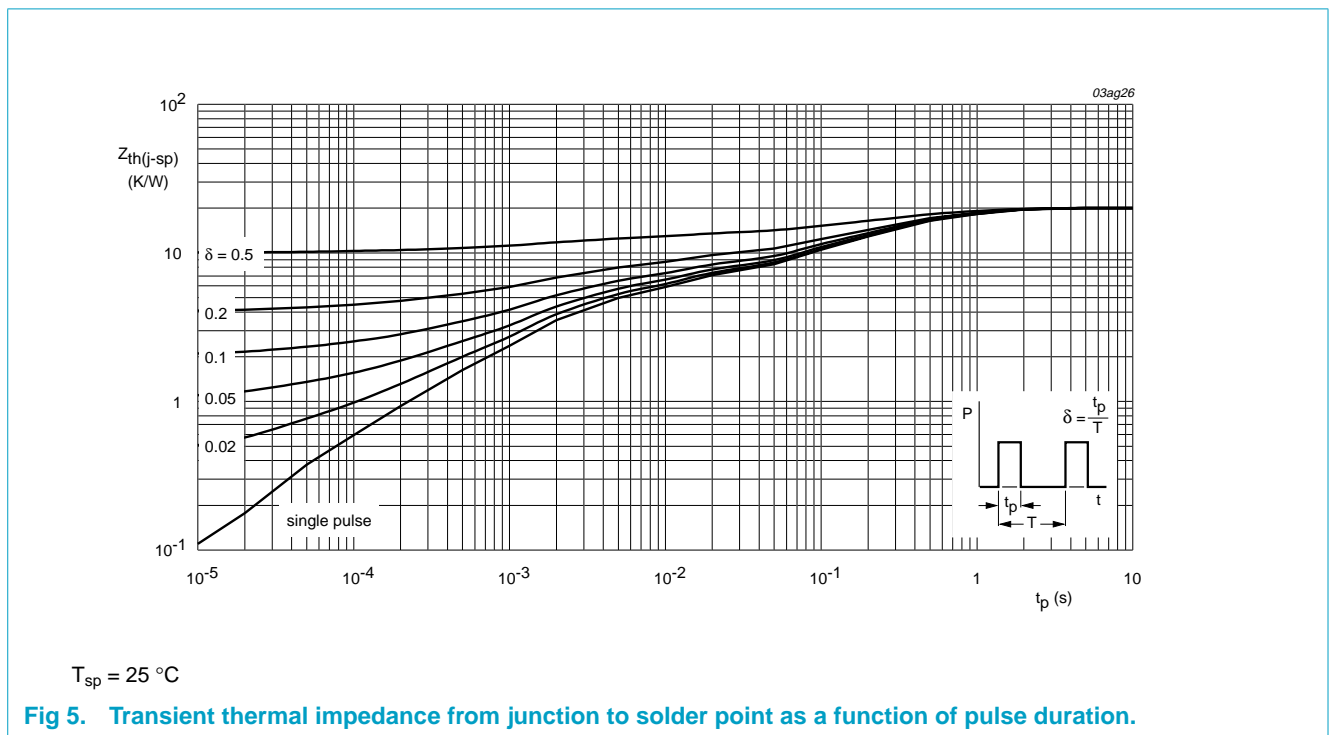
Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 5	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	150	K/W

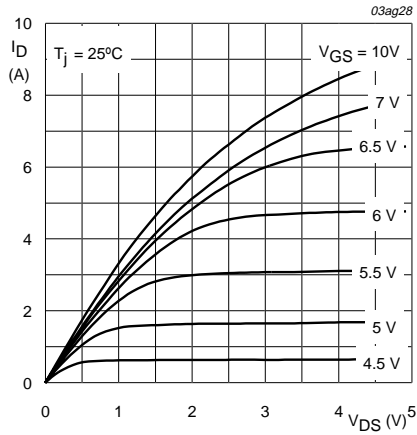
7.1 Transient thermal impedance



8. Characteristics

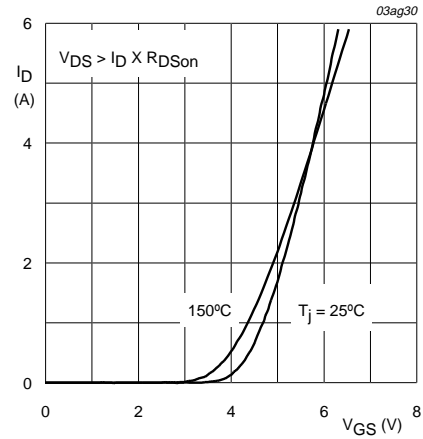
Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ }^\circ\text{C}$	100	120	–	V
		$T_j = -55\text{ }^\circ\text{C}$	89	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 10 $T_j = 25\text{ }^\circ\text{C}$	2	3	4	V
		$T_j = 150\text{ }^\circ\text{C}$	1.2	–	–	V
		$T_j = -55\text{ }^\circ\text{C}$	–	–	6	V
I_{DSS}	drain-source leakage current	$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ }^\circ\text{C}$	–	1	25	μA
		$T_j = 150\text{ }^\circ\text{C}$	–	4	250	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\ \text{V}$; $V_{DS} = 0\ \text{V}$	–	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 1.75\ \text{A}$; Figure 8 and 9 $T_j = 25\text{ }^\circ\text{C}$	–	315	430	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	–	725	990	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 5\ \text{V}$; $I_D = 2.5\ \text{A}$	–	3	–	S
$Q_{g(tot)}$	total gate charge	$I_D = 2.5\ \text{A}$; $V_{DD} = 80\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 14	–	5.1	–	nC
Q_{gs}	gate-source charge		–	1	–	nC
Q_{gd}	gate-drain (Miller) charge		–	2.1	–	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 12	–	160	–	pF
C_{oss}	output capacitance		–	29	–	pF
C_{rss}	reverse transfer capacitance		–	18	–	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\ \text{V}$; $R_D = 27\ \Omega$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$	–	4.5	–	ns
t_r	rise time		–	7.7	–	ns
$t_{d(off)}$	turn-off delay time		–	7.8	–	ns
t_f	fall time		–	2.5	–	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 2.5\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 13	–	0.9	1.5	V
t_{rr}	reverse recovery time	$I_S = 2.5\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	–	45	–	ns
Q_r	recovered charge		–	90	–	nC



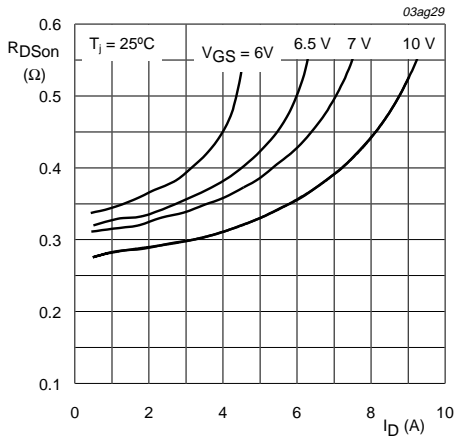
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



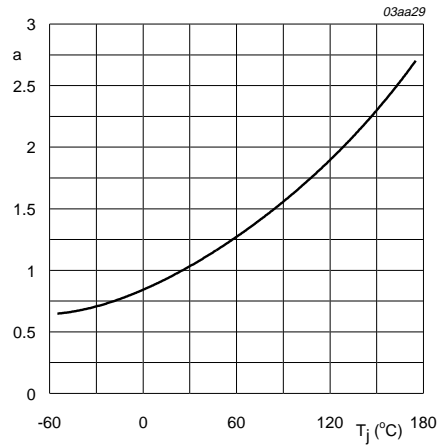
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



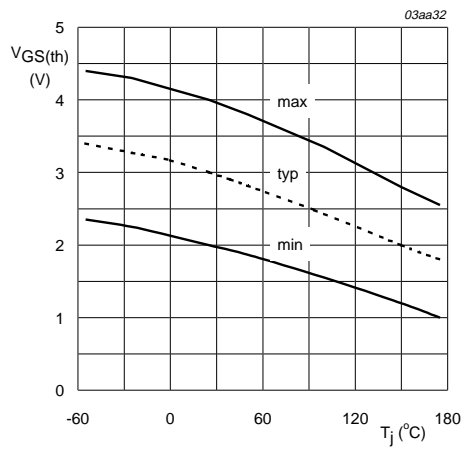
$T_j = 25^\circ\text{C}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



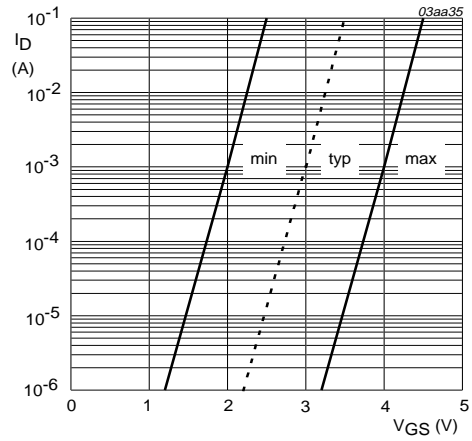
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



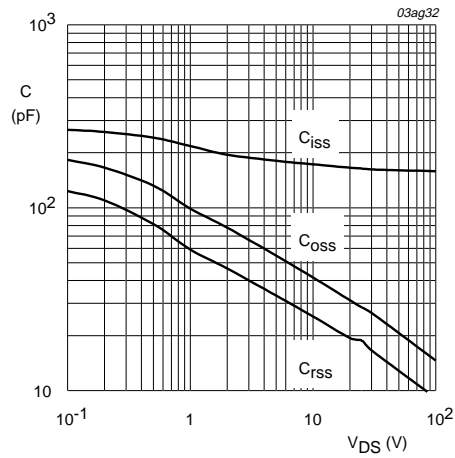
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



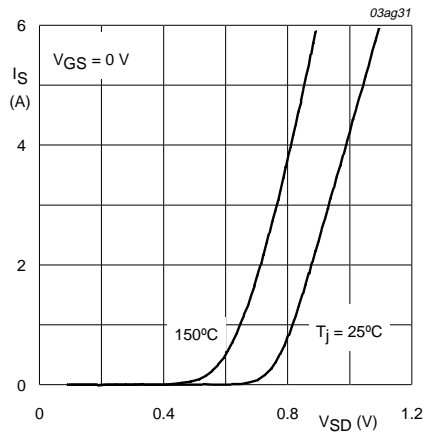
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 10 \text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



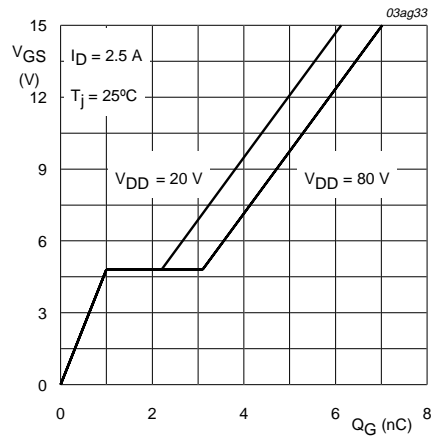
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0$ V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 2.5$ A; $V_{DD} = 80$ V, 20V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223

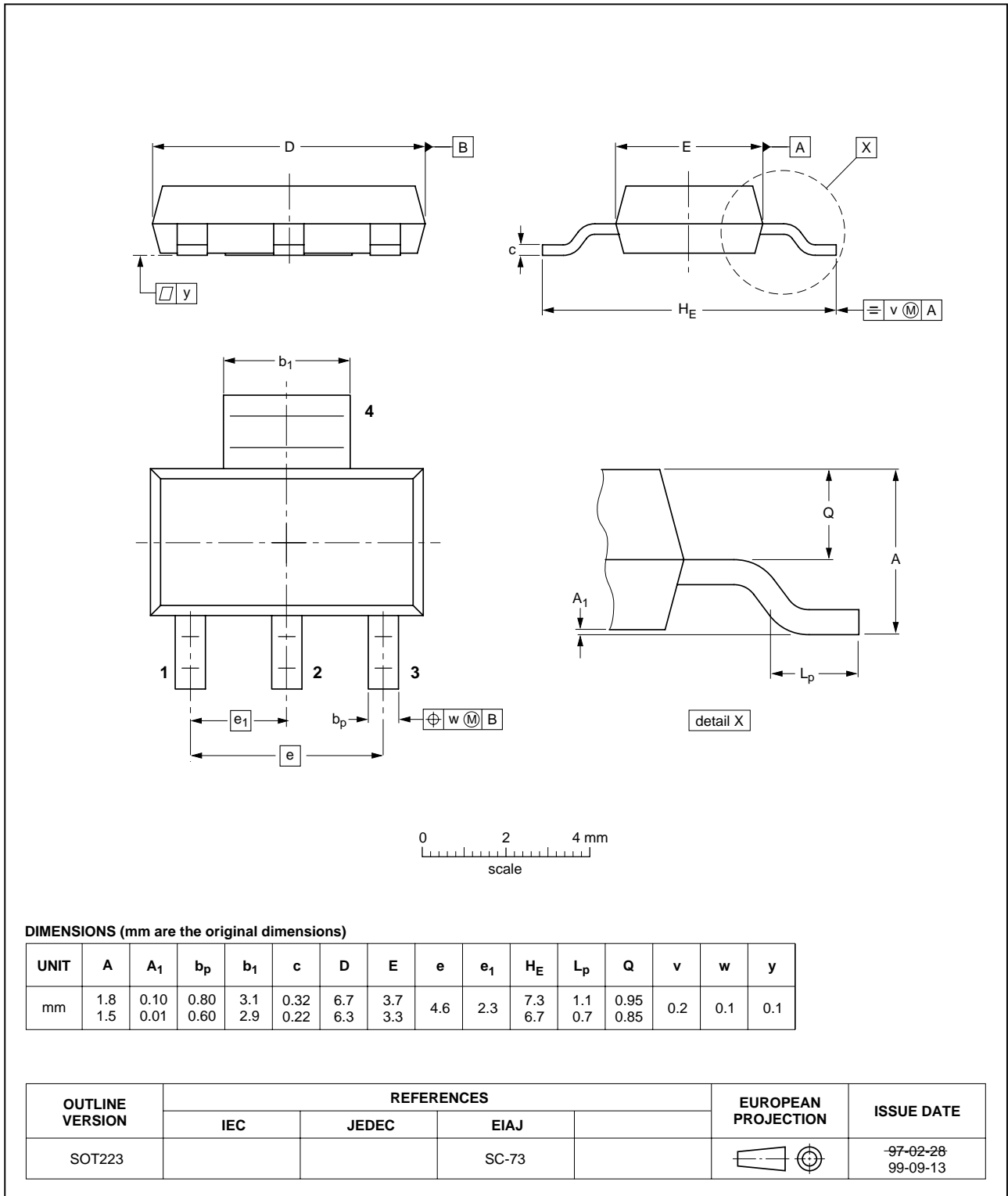


Fig 15. SOT223.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20001016	-	Product specification; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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