Advance Information

MPC860TS/D
Rev. 0.1, 11/2001

MPC860 PowerQUICC
Technical Summary

The MPC860 Quad Integrated Communications Controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in both communications and networking systems. Unless otherwise specified, the PowerQUICC unit is referred to as the MPC860 in this manual.

The MPC860 is a PowerPC architecture-based derivative of Motorola's MC68360 Quad Integrated Communications Controller (QUICC™). The CPU on the MPC860 is a 32-bit MPC8xx core implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. Digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

The purpose of this manual is to describe the operation of all the MPC860 functionality with concentration on the I/O functions. Additional information can be found in *Programming Environments Manual for the PowerPC Architecture.*

1.1 Features

The following list summarizes the key MPC860 features:

- Embedded MPC8xx core
- Single issue, 32-bit version of the core (compatible with the PowerPC architecture definition) with 32, 32-bit general-purpose registers (GPRs)
  - — The core performs branch prediction with conditional prefetch, without conditional execution
  - — 4-Kbyte data cache and 4-Kbyte instruction cache
  - — Instruction and data caches are two-way, set-associative, physical address, least recently used (LRU) replacement, lockable on-line granularity
  - — MMUs with 32 entry TLB, fully associative instruction and data TLBs
  - — MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16

virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Complete static design
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer and time base
  - Real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)

  - Up to 384 buffer descriptors (BDs)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 5 Kbytes of dual-port RAM
  - 16 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Four SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation (Available only on specially programmed devices)
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C (inter-integrated circuit) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, clocking
  - Allows dynamic changes

  - Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC860 or MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported
- Low power support
  - Full on—All units fully powered
  - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
  - Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
  - Power down mode— All units powered down except PLL, RTC, PIT, time base and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports Conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility
- 357-pin ball grid array (BGA) package

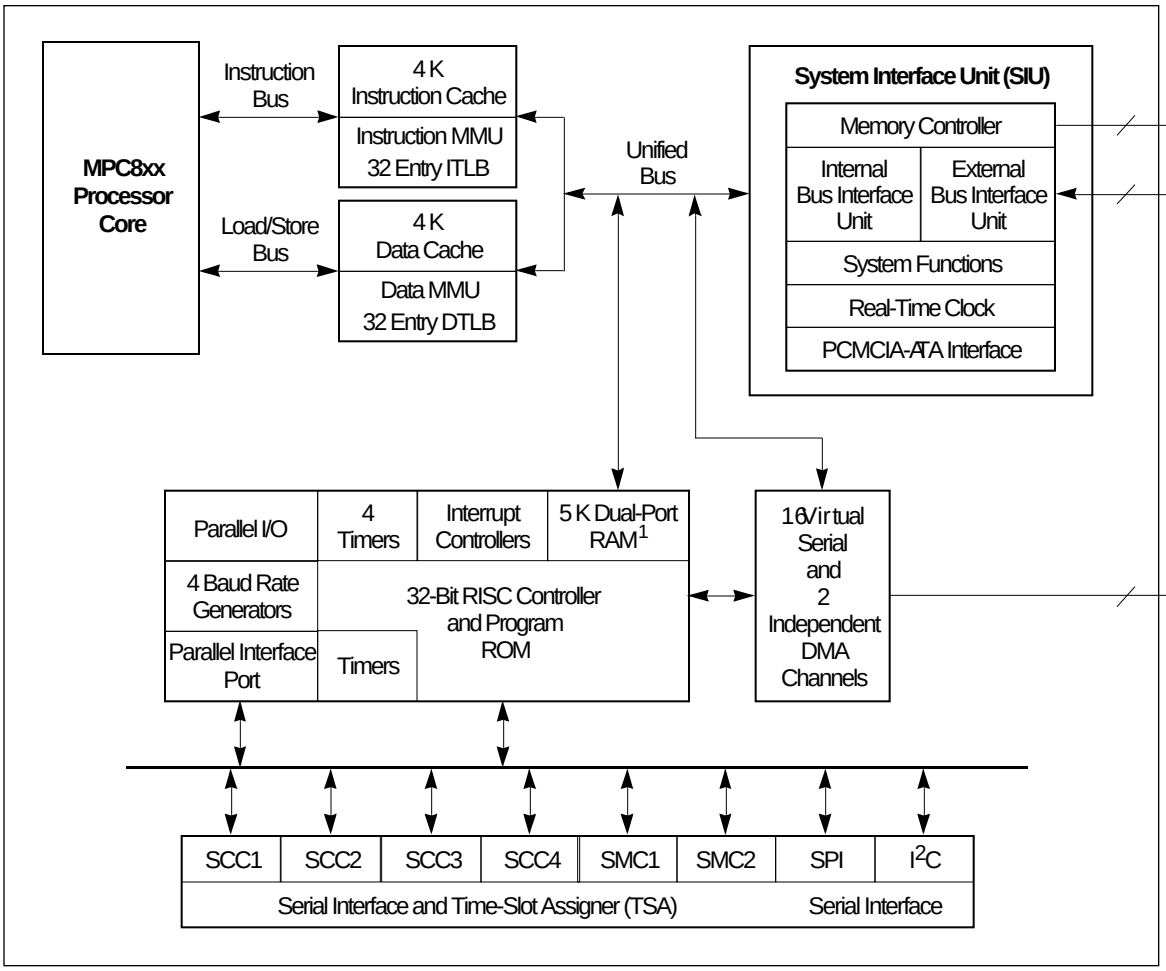

Figure 1. MPC860 Block Diagram

1.2 Architecture Overview

The MPC860 integrates an embedded MPC8xx core with high-performance, low-power peripherals to extend the Motorola Data Communications family of embedded processors even farther into high-end communications and networking products.

The MPC860 is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC860 block diagram is shown in Figure 1.

1.3 Embedded MPC8xx Core

The core is compliant with the UISA (user instruction set architecture) portion of the PowerPC architecture. It is a fully static design that has an integer unit (IU) and a load/store unit (LSU). It executes all integer and load/store operations in hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core can operate on 32-bit external operands with one bus cycle.

The IU uses 32, 32-bit GPRs for source and target operands. Typically, it can execute one integer instruction each clock cycle. Each element in the integer block is clocked only when valid data is present in the data queue ready for operation. This assures that power consumption of the device is held to the absolute minimum required for operation.

The core is integrated with MMUs as well as 4-Kbyte instruction and data caches. Each MMU provides a 32 entry, fully associative instruction and data TLB, with multiple page sizes of 4, 16, 512, and 256 Kbytes and 8 Mbytes. It supports 16 virtual address spaces with 8 protection groups. Three special scratch registers support software table walk and update.

The instruction cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hits with no added latency for misses. It has four words per block, supporting a four-beat burst line fill using an LRU (least recently used) replacement algorithm. The cache can be locked on a per cache block basis for application-critical routines.

The data cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle accesses on hits with one added clock latency for misses. It has four words per cache block, supporting burst line fill using LRU replacement. The cache can be locked on a per block basis for application critical routines. The data cache can be programmed to support copy-back or write-through via the MMU. The inhibit mode can be programmed per MMU page.

The core contains a much improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally it has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data address bus, and two comparators operating on the data bus. The core can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a break point that can be programmed to trigger in a programmable number of events.

1.4 System Interface Unit (SIU)

The SIU on the MPC860 integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC device.

Dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, reset control, decrementer, time base and the real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, flash EPROM, SRDRAM, EDO and other peripherals with two-clock access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–30 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte enable signals, one output enable signal and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256 or 512 Kbytes or 1, 2, 4, 8, 16, 32, or 64 Mbytes for all port sizes. In addition the memory depth can be defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC860 supports a glueless interface to one bank of DRAM while external buffers are required for additional

memory banks. The refresh unit provides $\overline{CAS}$ before $\overline{RAS}$, a programmable refresh timer, refresh active during external reset, disable refresh mode, and stacking up to 7 refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

1.5 PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides 8 memory or I/O windows where each window can be allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

1.6 Power Management

The MPC860 supports a wide range of power management features including full on, doze, sleep, deep sleep, and low power stop. In full on mode the MPC860 processor is fully powered with all internal units operating at the full speed of the processor. A gear mode is provided which is determined by a clock divider, allowing the operating system to reduce the operational frequency of the processor. Doze mode disables core functional units other than the time base decrementer, PLL, memory controller, RTC, and then places the CPM in low-power standby mode. Sleep mode disables everything except the RTC and PIT, leaving the PLL active for quick wake-up. Deep sleep mode disables the PLL for lower power but slower wake-up. Low-power stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

1.7 Communications Processor Module (CPM)

The MPC860 is the next generation MC68360 QUICC and like its predecessor implements a dual-processor architecture. This dual-processor architecture provides both a high-performance general purpose processor for application programming use as well as a special purpose communication processor (CPM) uniquely designed for communications needs.

The CPM contains features that allow the MPC860 to excel in communications and networking products as did the MC68360 QUICC which preceded it. These features may be divided into three sub-groups:

- Communications processor (CP)
- Sixteen independent DMA (SDMA) controllers
- Four general-purpose timers

The CP provides the communication features of the MPC860. Included are a RISC processor, two serial communication controllers (SCC), four serial management controllers (SMC), one serial peripheral interface (SPI), one I^2C interface, 5 Kbytes of dual-port RAM, an interrupt controller, a time-slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and sixteen serial DMA channels to support the SCCs, SMCs, SPI, and I^2C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer.

The MPC860 maintains the best features of the MC68360 QUICC, while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the PowerPC architecture. Because the CPM architectural approach remains intact between the MPC860 and the MC68360 QUICC, a user of the MC68360 QUICC can easily become familiar with the MPC860.

1.8 Software Compatibility Issues

The following list summarizes the major software differences between the MC68360 QUICC and the MPC860:

- Since the MPC860 is compliant with the PowerPC architecture, code written for the MC68360 must be recompiled for the PowerPC instruction set. Code that accesses MC68360 peripherals requires only minor modifications for use with the MPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different and therefore code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers that also support the PowerPC architecture.

When porting code from the MC68360 CPM to the MPC860 CPM, the software writer has new options for setting hardware break points on CPU commands, address, and serial request which are useful for software debugging. Support for single-step operation with all CPM registers visible further simplifies software development for the CPM.

Table 1. Revision History

Revision	Date	Change
0	3/1999	Initial document
0.1	11/2001	Template change, removed references to MAC functionality

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.;
SPS, Technical Information Center,
3-20-1, Minami-Azabu Minato-ku,
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.;
Silicon Harbour Centre, 2 Dai King Street,
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

DOCUMENT COMMENTS:

FAX (512) 933-2625,
Attn: RISC Applications Engineering

MPC860TS/D

Freescale Semiconductor, Inc.