M36DR432AD
M36DR432BD

32 Mbit (2Mb x16, Dual Bank, Page) Flash Memory and 4 Mbit (256Kb x16) SRAM, Multiple Memory Product

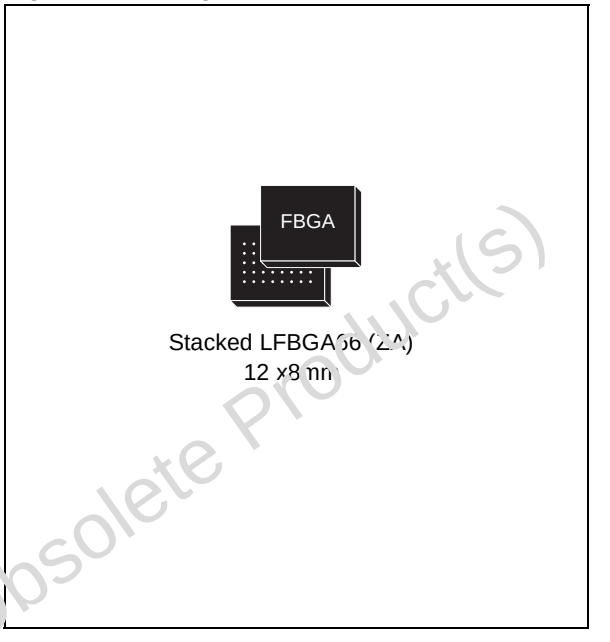
FEATURES SUMMARY

- Multiple Memory Product
  - 1 bank of 32 Mbit (2Mb x16) Flash Memory
  - 1 bank of 4 Mbit (256Kb x16) SRAM
- SUPPLY VOLTAGE
  - V_{DDF} = V_{DDS} =1.65V to 2.2V
  - V_{PPF} = 12V for Fast Program (optional)
- ACCESS TIMES: 85ns, 100ns, 120ns
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code, M36DR432AD: 00A0h
  - Bottom Device Code, M36DR432BD: 00A1h

FLASH MEMORY

- MEMORY BLOCKS
  - Dual Bank Memory Array: 4 Mbit, 28 Mbit
  - Parameter Blocks (Top or Bottom location)
- PROGRAMMING TIME
  - 10µs by Word typical
  - Double Word Program Option
- ASYNCHRONOUS PAGE MODE READ
  - Page Width: 4 Words
  - Page Access: 35ns
  - Random Access: 85ns, 100ns, 120ns
- DUAL BANK OPERATIONS
  - Read within one Bank while Program or Erase within the other
  - No delay between Read and Write operations
- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WPF}$ for Block Lock-Down
- COMMON FLASH INTERFACE (CFI)
  - 64 bit Unique Device Identifier
  - 64 bit User Programmable OTP Cells

Figure 1. Package



- ERASE SUSPEND and RESUME MODES
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year

SRAM

- 4 Mbit (256Kb x16)
- LOW V_{DDS} DATA RETENTION: 1.0V
- POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS

TABLE OF CONTENTS

SUMMARY DESCRIPTION 6

Figure 2. Logic Diagram 6
Table 1. Signal Names 6
Figure 3. TFBGA Connections (Top view through package) 7

SIGNAL DESCRIPTIONS 8

Address Inputs (A0-A17) 8
Address Inputs (A18-A20) 8
Data Input/Output (DQ0-DQ15) 8
Flash Chip Enable (EF) 8
Flash Output Enable (GF) 8
Flash Write Enable (WF) 8
Flash Write Protect (WPF) 8
Flash Write Protect (WPF) 8
Flash Reset/Power-Down (RPF) 8
VDDF Supply Voltage (1.65V to 2.2V) 8
V_{PPF} Programming Voltage (11.4V to 12.6V) 8
V_{SSF} Ground 8
SRAM Chip Enable (ES) 8
SRAM Write Enable (WS) 9
SRAM Output Enable (GS) 9
SRAM Upper Byte Enable (UBS) 9
SRAM Lower Byte Enable (LBS) 9
VDDS Supply Voltage (1.65V to 2.2V) 9

FUNCTIONAL DESCRIPTION 10

Figure 4. Functional Block Diagram 10
Table 2. Main Operation Modes 11

FLASH MEMORY COMPONENT 12

Table 3. Flash Bank Architecture 12
Figure 5. Flash Security Block and Protection Register Memory Map 13

Flash Bus Operations 13
Flash Read 13
Flash Write 13
Flash Output Disable 13
Flash Standby 13
Automatic Flash Standby 13
Flash Power-Down 13
Dual Bank Operations 13

Flash Command Interface 13
Flash Read/Reset Command 14
Flash Read CFI Query Command 14

Auto Select Command. . . . 14
Set Configuration Register Command. . . . 14
Program Command. . . . 14
Double Word Program Command. . . . 14
Quadruple Word Program Command. . . . 14
Enter Bypass Mode Command. . . . 15
Exit Bypass Mode Command. . . . 15
Program in Bypass Mode Command. . . . 15
Double Word Program in Bypass Mode Command. . . . 15
Quadruple Word Program in Bypass Mode Command. . . . 15
Block Lock Command 15
Block Unlock Command 15
Block Lock-Down Command 15
Block Erase Command. . . . 15
Bank Erase Command. . . . 16
Erase Suspend Command. . . . 16
Erase Resume Command. . . . 16
Protection Register Program Command 16
Table 4. Flash Commands 17
Table 5. Read Electronic Signature 18
Table 6. Flash Read Block Protection 18
Table 7. Configuration Register 18
Table 8. Read Protection Register 19
Table 9. Program, Erase Times and Program, Erase Endurance Cycles 19

Flash Block Locking 19
Reading a Block's Lock Status 19
Locked State 20
Unlocked State 20
Lock-Down State 20
Locking Operations During Erase Suspend 20
Table 10. Flash Lock Status 21

Flash Status Register 21
Data Polling Bit (DQ7). . . . 21
Toggle Bit (DQ6). . . . 21
Toggle Bit (DQ2). . . . 21
Error Bit (DQ5). . . . 22
Erase Timer Bit (DQ3). . . . 22
Polling and Toggle Bits 22
Table 11. Polling and Toggle Bits 22
Table 12. Status Register Bits 23

SRAM COMPONENT 24

SRAM Operations 24
Read 24
Write 24

Standby/Power-Down . . . 24
Data Retention . . . 24
Output Disable . . . 24

MAXIMUM RATING . . . 25

Table 13. Absolute Maximum Ratings(1) . . . 25

DC AND AC PARAMETERS . . . 26

Table 14. Operating and AC Measurement Conditions . . . 26
Figure 6. AC Measurement I/O Waveform . . . 26
Figure 7. AC Measurement Load Circuit . . . 26
Table 15. Device Capacitance . . . 26
Table 16. Flash DC Characteristics . . . 27
Table 17. SRAM DC Characteristics (T_A = –40 to 85°C; V_{DDF} = V_{DDS} = 1.65V to 2.2V) . . . 28
Figure 8. Flash Random Read AC Waveforms . . . 29
Figure 9. Flash Page Read AC Waveforms . . . 30
Table 18. Flash Read AC Characteristics . . . 31
Figure 10. Flash Write AC Waveforms, Write Enable Controlled . . . 32
Table 19. Flash Write AC Characteristics, Write Enable Controlled . . . 32
Figure 11. Flash Write AC Waveforms, Chip Enable Controlled . . . 33
Table 20. Flash Write AC Characteristics, Chip Enable Controlled . . . 33
Figure 12. Flash Reset/Power-Down AC Waveform . . . 34
Table 21. Flash Reset/Power-Down AC Characteristics . . . 34
Figure 13. Flash Data Polling DQ7 AC Waveforms . . . 35
Figure 14. Flash Data Toggle DQ6, DQ2 AC Waveforms . . . 36
Table 22. Flash Data Polling and Toggle Bits AC Characteristics . . . 37
Figure 15. Flash Data Polling Flowchart . . . 37
Figure 16. Flash Data Toggle Flowchart . . . 37
Figure 17. SRAM Read Mode AC Waveforms, Address Controlled with UBS = LBS = V_{IL} . . . 38
Figure 18. SRAM Read AC Waveforms, ES or GS Controlled . . . 38
Figure 19. SRAM Standby AC Waveforms . . . 39
Table 23. SRAM Read AC Characteristics) . . . 39
Figure 20. SRAM Write AC Waveforms, WS Controlled with GS Low . . . 40
Figure 21. SRAM Write AC Waveforms, WS Controlled with GS High . . . 40
Figure 22. SRAM Write Cycle Waveform, UBS and LBS Controlled, G Low . . . 41
Figure 23. SRAM Write AC Waveforms, ES Controlled . . . 41
Table 24. SRAM Write AC Characteristics . . . 42
Figure 24. SRAM Low V_{DDS} Data Retention AC Waveforms, ES Controlled . . . 42
Table 25. SRAM Low V_{DDS} Data Retention Characteristics (1, 2) . . . 43

PACKAGE MECHANICAL . . . 44

Figure 25. Stacked LFBGA 12x8mm - 8x8 ball array, 0.8mm pitch, Bottom View Package Outline 44
Table 26. Stacked LFBGA 12x8mm - 8x8 ball array, 0.8mm pitch, Package Mechanical Data . . . 44

PART NUMBERING 45

Table 27. Ordering Information Scheme 45

APPENDIX A. BLOCK ADDRESSES 46

Table 28. Bank A, Top Boot Block Addresses M36DR432AD 46
Table 29. Bank B, Top Boot Block Addresses M36DR432AD 46
Table 30. Bank B, Bottom Boot Block Addresses M36DR432BD 47
Table 31. Bank A, Bottom Boot Block Addresses M36DR432BD 47

APPENDIX B. COMMON FLASH INTERFACE 48

Table 32. Query Structure Overview 48
Table 33. CFI Query Identification String 48
Table 34. CFI Query System Interface Information 49
Table 35. Device Geometry Definition 50

REVISION HISTORY 51

Table 36. Document Revision History 51

SUMMARY DESCRIPTION

The M36DR432AD/BD is a low-voltage Multiple Memory Product which combines two memory devices: a 32 Mbit (2Mbit x16) non-volatile Flash memory and a 4 Mbit SRAM.

The memory is available in a Stacked LFBGA66 12x8mm - 8x8 active ball array, 0.8mm pitch package and supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

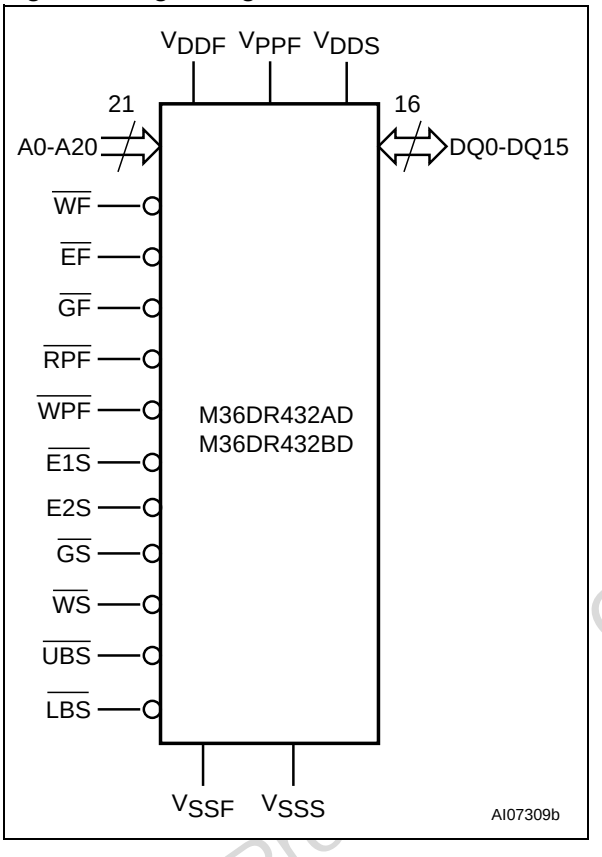
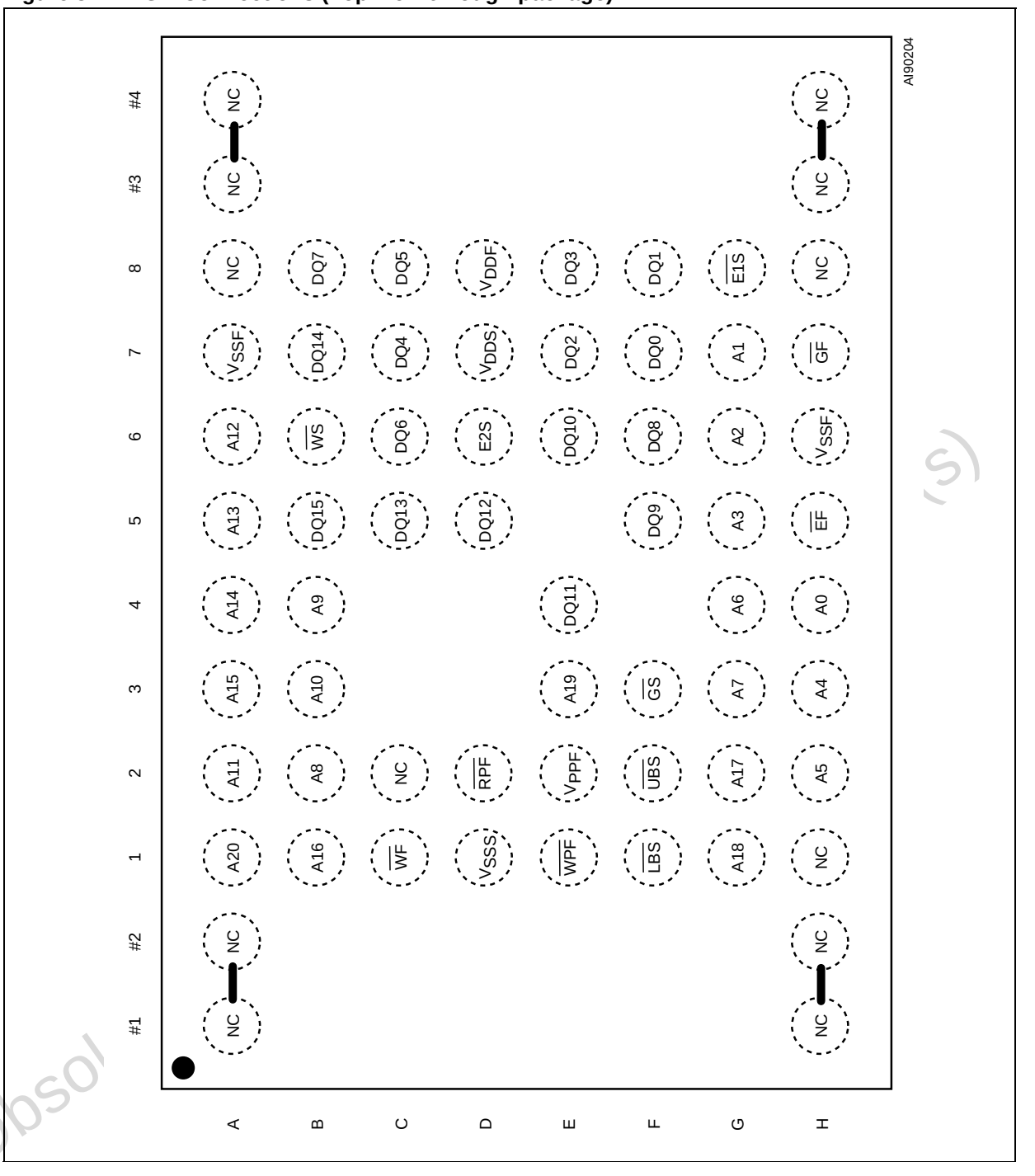


Table 1. Signal Names

A0-A17	Address Inputs
A18-A20	Address Inputs for Flash Chip only
DQ0-DQ15	Data Input/Outputs, Command Inputs
V_{DDF}	Flash Power Supply
V_{PPF}	Flash Optional Supply Voltage for Fast Program & Erase
V_{SSF}	Flash Ground
V_{DDS}	SRAM Power Supply
V_{SSS}	SRAM Ground
NC	Not Connected Internally
Flash control functions	
$\overline{EF}$	Chip Enable
$\overline{GF}$	Output Enable
$\overline{WF}$	Write Enable
$\overline{RPF}$	Reset/Power-Down
$\overline{WPF}$	Write Protect input
SRAM control functions	
$\overline{E1S}$	Chip Enable
E2S	Chip Enable
$\overline{GS}$	Output Enable
$\overline{WS}$	Write Enable
$\overline{UBS}$	Upper Byte Enable
$\overline{LBS}$	Lower Byte Enable

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A17). Addresses A0-A17 are common inputs for the Flash and the SRAM components. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. During a write operation, the address inputs for the Flash memory are latched on the falling edge of the Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{WF}$), whichever occurs last, whereas for the SRAM array they are latched on the falling edge of the SRAM Chip Enable lines ($\overline{E1S}$ or E2S) or Write Enable ($\overline{WS}$). In the rest of the datasheet, only the Active Low SRAM Chip Enable line will be discussed. It will be referred to as $\overline{ES}$.

Address Inputs (A18-A20). Addresses A18-A20 are inputs for the Flash component only. They are latched during a write operation on the falling edge of Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{WF}$), whichever occurs last.

Data Input/Output (DQ0-DQ15). The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Write Bus operation.

The input is data to be programmed in the Flash or SRAM memory array or a command to be written to the C.I. of the Flash memory. Both are latched on the rising edge of Flash Write Enable ($\overline{WF}$) and, SRAM Chip Enable lines ($\overline{ES}$) or Write Enable ($\overline{WS}$). The output is data from the Flash memory array or SRAM array, the Electronic Signature Manufacturer or Device codes, the Block Protection status, the Configuration Register status or the Status Register Data (Polling bit DQ7, Toggle bits DQ6 and DQ2, Error bit DQ5 or Erase Timer bit DQ3) depending on the address. Outputs are valid when Flash Chip Enable ($\overline{EF}$) and Output Enable ($\overline{GF}$) or SRAM Chip Enable lines ($\overline{ES}$) and Output Enable ($\overline{GS}$) are active.

The output is high impedance when both the Flash chip and the SRAM chip are deselected or the outputs are disabled and when Reset ($\overline{RPF}$) is at V_{IL}.

Flash Chip Enable ($\overline{EF}$). The Chip Enable input activates the Flash memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IH} the memory is deselected and the power consumption is reduced to the standby level.

Flash Output Enable ($\overline{GF}$). gates the outputs through the data buffers during a read operation. When Output Enable, $\overline{GF}$, is at V_{IH} the outputs are High impedance.

Flash Write Enable ($\overline{WF}$). The Write Enable controls the Bus Write operation of the Flash memory's Command Interface.

Flash Write Protect ($\overline{WPF}$). Write Protect is an input that gives an additional hardware protection for each Flash block. When Write Protect is at V_{IL}, the locked-down blocks cannot be locked or unlocked. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. Refer to Table 8, Read Protection Register.

Flash Reset/Power-Down ($\overline{RPF}$). The Reset/Power-Down input provides hardware reset of the Flash memory, and/or Power-Down functions, depending on the Flash Configuration Register status. Reset or Power-Down of the memory is achieved by pulling $\overline{RPF}$ to V_{IL} for at least t_{PLPH}.

The Reset/Power-Down function is set in the Configuration Register (see Set Configuration Register Command). If it is set to '0' the Reset function is enabled, if it is set to '1' the Power-Down function is enabled. After a Reset or Power-Up the power save function is disabled and all blocks are locked.

The memory Command Interface is reset on Power Up to Read Array. Either Chip Enable or Write Enable must be tied to V_{IH} during Power Up to allow maximum security and the possibility to write a command on the first rising edge of Write Enable.

After a Reset, when the device is in Read, Erase Suspend Read or Standby, valid data will be output t_{PHQ7V1} after the rising edge of $\overline{RPF}$. If the device is in Erase or Program, the operation will be aborted and the reset recovery will take a maximum of t_{PLQ7V}. The memory will recover from Reset/Power-Down t_{PHQ7V2} after the rising edge of $\overline{RPF}$. See Tables 18 and 19, and Figure 12.

V_{DDF} Supply Voltage (1.65V to 2.2V). V_{DDF} provides the power supply to the internal core and I/O pins of the memory device. It is the main power supply for all operations (read, program and erase).

V_{PPF} Programming Voltage (11.4V to 12.6V). V_{PPF} provides a high voltage power supply for fast factory programming. V_{PPF} is required to use the Double Word and Quadruple Word Program commands.

V_{SSF} Ground. V_{SSF} ground is the reference for the core supply. It must be connected to the system ground.

SRAM Chip Enable ($\overline{ES}$). The Chip Enable inputs for SRAM activate the memory control logic, input buffers and decoders. $\overline{ES}$ at V_{IH} deselects

the memory and reduces the power consumption to the standby level. $\overline{ES}$ can also be used to control writing to the SRAM memory array, while $\overline{WS}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL} and $\overline{ES}$ at V_{IL} at the same time.

SRAM Write Enable ($\overline{WS}$). The Write Enable input controls writing to the SRAM memory array. $\overline{WS}$ is active Low.

SRAM Output Enable ($\overline{GS}$). The Output Enable gates the outputs through the data buffers during a read operation of the SRAM chip. $\overline{GS}$ is active Low.

SRAM Upper Byte Enable ($\overline{UBS}$). Enables the upper bytes for SRAM (DQ8-DQ15). $\overline{UBS}$ is active Low.

SRAM Lower Byte Enable ($\overline{LBS}$). Enables the lower bytes for SRAM (DQ0-DQ7). $\overline{LBS}$ is active Low.

V_{DDS} Supply Voltage (1.65V to 2.2V). V_{DDS} is the SRAM power supply for all operations.

Note: Each device in a system should have V_{DDF} and V_{PPF} decoupled with a 0.1µF capacitor close to the pin. See Figure 7, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The Flash and SRAM components have separate power supplies and grounds and are distinguished by three chip enable inputs: $\overline{EF}$ for the Flash memory and $\overline{ES}$ ($\overline{E1S}$ and E2S, respectively) for the SRAM.

Figure 4. Functional Block Diagram

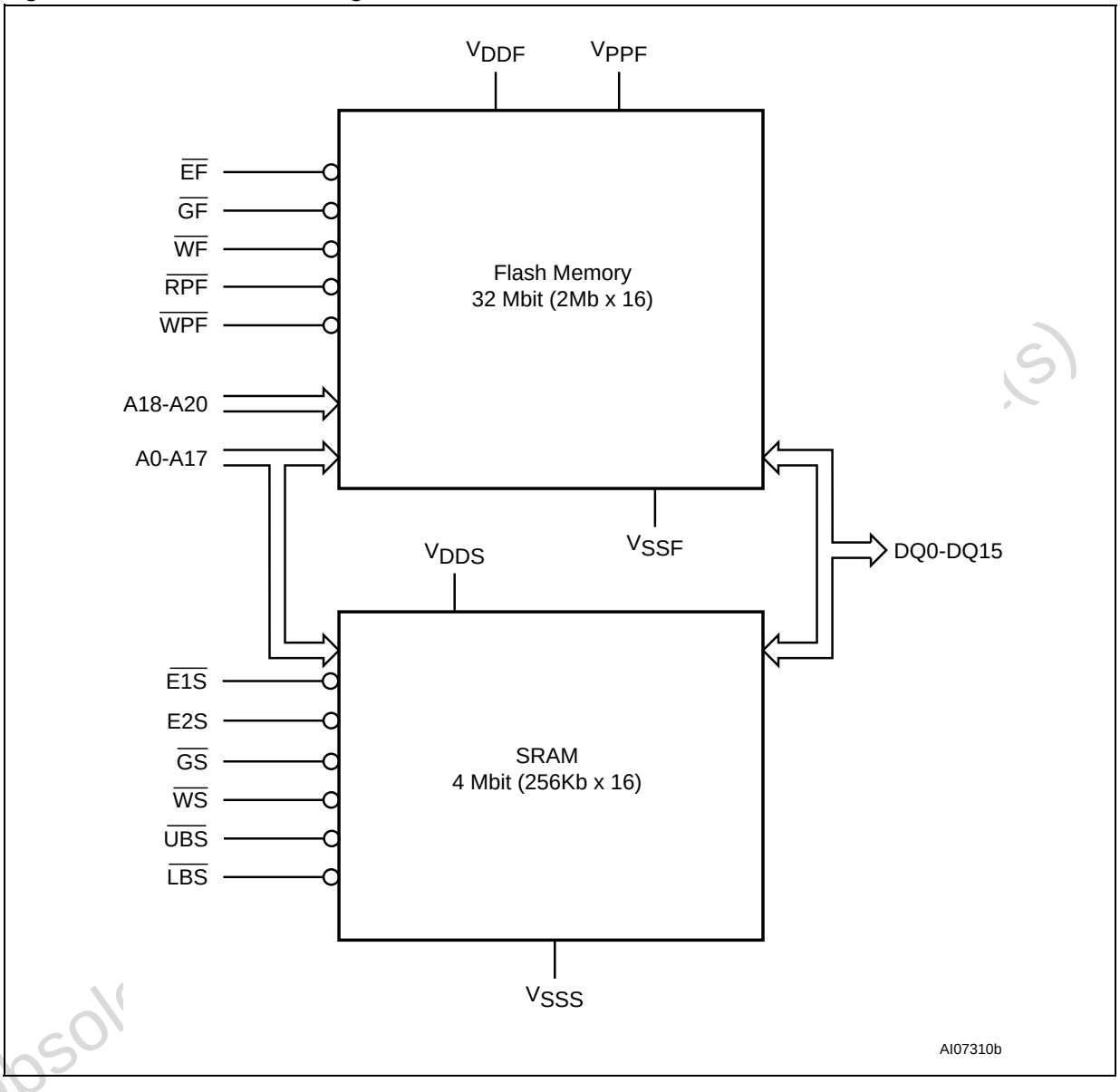


Table 2. Main Operation Modes

Operation Mode		$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	$\overline{RPF}$	$\overline{WPF}$	$\overline{ES}$	$\overline{GS}$	$\overline{WS}$	$\overline{UBS}$, $\overline{LBS}$(1)	DQ15-DQ0
Flash Memory	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	SRAM must be disabled				Data Output
	Page Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	SRAM must be disabled				Data Output
	Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	SRAM must be disabled				Data Input
	Standby	V_{IH}	X	X	V_{IH}	V_{IH}	Any SRAM mode is allowed				Hi-Z
	Reset/ Power-Down	X	X	X	V_{IL}	V_{IH}	Any SRAM mode is allowed				Hi-Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Any SRAM mode is allowed				Hi-Z
SRAM	Read	Flash must be disabled					V_{IL}	V_{IL}	V_{IH}	V_{IL}	Data out Word Read
	Write	Flash must be disabled					V_{IL}	V_{IH}	V_{IL}	V_{IL}	Data in Word Write
	Standby/Power Down	Any Flash mode is allowable					V_{IH}	X	X	X	Hi-Z
							X	X	X	V_{IH}	Hi-Z
	Data Retention	Any Flash mode is allowable					V_{IH}	X	X	X	Hi-Z
							X	X	X	V_{IH}	Hi-Z
	Output Disable	Any Flash mode is allowable					V_{IL}	V_{IH}	V_{IH}	X	Hi-Z

Note: 1. X = Don't care (V_{IL} or V_{IH}).
2. If $\overline{UBS}$ and $\overline{LBS}$ are tied together the bus is at 16 bit. For an 8 bit bus configuration use $\overline{UBS}$ and $\overline{LBS}$ separately.

FLASH MEMORY COMPONENT

The Flash Memory is a 32 Mbit (2Mbit x16) non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.2V V_{DDF} supply for the circuitry and a 1.65V to 2.2V V_{DDQF} supply for the Input/Output pins (in the stacked device, V_{DDF} and V_{DDQF} are tied internally). An optional 12V V_{PPF} power supply is provided to speed up customer programming.

The Flash device features an asymmetrical block architecture with an array of 71 blocks divided into two banks, Banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible in Bank B or vice versa. Only one bank at a time is allowed to be in program or erase mode. The bank architecture is summarized in Table 3, and the Block Addresses are shown in Appendix A. The Parameter Blocks are located at the top of the memory address space for the M36DR432AD and, at the bottom for the M36DR432BD.

Each block can be erased separately. Erase can be suspended, in order to perform either read or program in any other block, and then resumed. Each block can be programmed and erased over 100,000 cycles.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

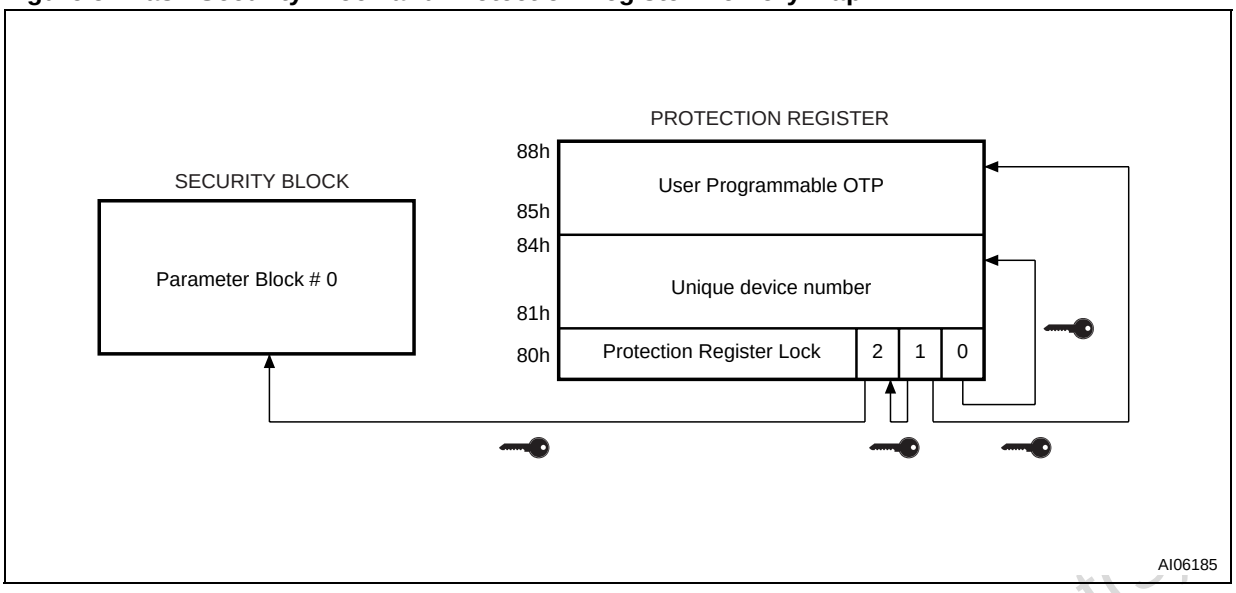
The Flash memory features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have two levels of protection. They can be individually locked and locked-down preventing any accidental programming or erasure. All blocks are locked at Power Up and Reset.

The device includes a 128 bit Protection Register and a Security Block to increase the protection of a system's design. The Protection Register is divided into two 64 bit segments. The first segment contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user. Figure 5, shows the Flash Security Block and Protection Register Memory Map.

Table 3. Flash Bank Architecture

	Bank Size	Parameter Blocks	Main Blocks
Bank A	4 Mbits	8 blocks of 4 KWords	7 blocks of 32 KWords
Bank B	28 Mbits	-	56 blocks of 32 KWords

Figure 5. Flash Security Block and Protection Register Memory Map



Flash Bus Operations

The following operations can be performed using the appropriate bus cycles: Flash Read Array (Random and Page Modes), Flash Write, Flash Output Disable, Flash Standby and Flash Reset/ Power-Down, see Table 2, Main Operation Modes.

Flash Read. Flash Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the CFI, the Block Protection Status or the Configuration Register status. Read operation of the Flash memory array is performed in asynchronous page mode, that provides fast access time. Data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by A0-A1 address inputs. Read operations of the Electronic Signature, the Status Register, the CFI, the Block Protection Status, the Configuration Register status and the Security Code are performed as single asynchronous read cycles (Random Read). Both Flash Chip Enable $\overline{EF}$ and Flash Output Enable $\overline{GF}$ must be at V_{IL} in order to read the output of the memory.

Flash Write. Write operations are used to give commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{EF}$ and Write Enable $\overline{WF}$ are at V_{IL} with Output Enable $\overline{GF}$ at V_{IH}. Addresses are latched on the falling edge of $\overline{WF}$ or $\overline{EF}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{WF}$ or $\overline{EF}$ whichever occurs first. Noise pulses of less than 5ns typical on $\overline{EF}$, $\overline{WF}$ and $\overline{GF}$ signals do not start a write cycle.

Flash Output Disable. The data outputs are high impedance when the Output Enable $\overline{GF}$ is at V_{IH} with Write Enable $\overline{WF}$ at V_{IH}.

Flash Standby. The memory is in standby when Chip Enable $\overline{EF}$ is at V_{IH} and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{GF}$ or Write Enable $\overline{WF}$ inputs.

Automatic Flash Standby. In Read mode, after 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus.

Flash Power-Down. The memory is in Power-Down when the Configuration Register is set for/ Power-Down and $\overline{RPF}$ is at V_{IL}. The power consumption is reduced to the Power-Down level, and Outputs are high impedance, independent of the Chip Enable $\overline{EF}$, Output Enable $\overline{GF}$ or Write Enable $\overline{WF}$ inputs.

Dual Bank Operations. The Dual Bank allows data to be read from one bank of memory while a program or erase operation is in progress in the other bank of the memory. Read and Write cycles can be initiated for simultaneous operations in different banks without any delay. Status Register during Program or Erase must be monitored using an address within the bank being modified.

Flash Command Interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller han-

dles all timings and verifies the correct execution of the Program and Erase commands. Two bus write cycles are required to unlock the Command Interface. They are followed by a setup or confirm cycle. The increased number of write cycles is to ensure maximum data security.

The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface is reset to Read mode when power is first applied or exiting from Reset. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode

Flash Read/Reset Command. The Read/Reset command returns the device to Read mode. One Bus Write cycle is required to issue the Read/Reset command and return the device to Read mode. Subsequent Read operations will read the addressed location and output the data. The write cycle can be preceded by the unlock cycles but it is not mandatory.

Flash Read CFI Query Command. The Read CFI Query command is used to read data from the Common Flash Interface (CFI) and the Electronic Signature (Manufacturer or the Device Code, see Table 5). The Read CFI Query Command consists of one Bus Write cycle. Once the command is issued the device enters Read CFI mode. Subsequent Bus Read operations read the Common Flash Interface or Electronic Signature. Once the device has entered Read CFI mode, only the Read/Reset command should be used and no other. Issuing the Read/Reset command returns the device to Read mode.

See Appendix B, Common Flash Interface, Tables 33, 34, and 35 for details on the information contained in the Common Flash Interface memory area.

Auto Select Command. The Auto Select command uses the two unlock cycles followed by one write cycle to any bank address to setup the command. Subsequent reads at any address will output the Block Protection status, Protection Register and Protection Register Lock or the Configuration Register status depending on the levels of A0 and A1 (see Tables 6, 7 and 8). Once the Auto Select command has been issued only the Read/Reset command should be used and no other. Issuing the Read/Reset command returns the device to Read mode.

Set Configuration Register Command. The Flash component contains a Configuration Register, see Table 7, Configuration Register.

It is used to define the status of the Reset/Power-Down functions. The value for the Configuration Register is always presented on A0-A15, the other address bits are ignored. Address input A10 defines the status of the Reset/Power-Down functions. If it is set to '0' the Reset function is enabled, if it is set to '1' the Power-Down function is enabled. At Power Up the Configuration Register bit is set to '0'.

The Set Configuration Register command is used to write a new value to the Configuration Register. The command uses the two unlock cycles followed by one write cycle to setup the command and a further write cycle to write the data and confirm the command.

Program Command. The Program command uses the two unlock cycles followed by a write cycle to setup the command and a further write cycle to latch the Address and Data and start the Program Erase Controller. Read operations within the same bank output the Status Register after programming has started.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1', only if V_{PPF} is in the range of 11.4V to 12.6V.

Double Word Program Command. This feature is offered to improve the programming throughput by writing a page of two adjacent words in parallel. The V_{PPF} supply voltage is required to be from 11.4V to 12.6V for the Double Word Program command.

The command uses the two unlock cycles followed by a write cycle to setup the command. A further two cycles are required to latch the address and data of the two Words and start the Program Erase Controller.

The addresses must be the same except for the A0. The Double Word Program command can be executed in Bypass mode to skip the two unlock cycles.

Note that the Double Word Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Double Word Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1'.

Quadruple Word Program Command. The Quadruple Word Program command improves the programming throughput by writing a page of four adjacent words in parallel. The four words must differ only for the addresses A0 and A1. The V_{PPF} supply voltage is required to be from 11.4V to 12.6V for the Quadruple Word Program command.

The command uses the two unlock cycles followed by a write cycle to setup the command. A further four cycles are required to latch the address and data of the four Words and start the Program Erase Controller.

The Quadruple Word Program command can be executed in Bypass mode to skip the two unlock cycles.

Note that the Quadruple Word Program command cannot change a bit set to '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Quadruple Word Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1'.

Enter Bypass Mode Command. The Bypass mode is used to reduce the overall programming time when large memory arrays need to be programmed.

The Enter Bypass Mode command uses the two unlock cycles followed by one write cycle to set up the command. Once in Bypass mode, it is imperative that only the following commands be issued: Exit Bypass, Program, Double Word Program or Quadruple Word Program.

Exit Bypass Mode Command. The Exit Bypass Mode command uses two write cycles to setup and confirm the command. The unlock cycles are not required. After the Exit Bypass Mode command, the device resets to Read mode.

Program in Bypass Mode Command. The Program in Bypass Mode command can be issued when the device is in Bypass mode (issue a Enter Bypass Mode command). It uses the same sequence of cycles as the Program command with the exception of the unlock cycles.

Double Word Program in Bypass Mode Command. The Double Word Program in Bypass Mode command can be issued when the device is in Bypass mode (issue a Enter Bypass Mode command). It uses the same sequence of cycles as the Double Word Program command with the exception of the unlock cycles.

Quadruple Word Program in Bypass Mode Command. The Quadruple Word Program in Bypass Mode command can be issued when the device is in Bypass mode (issue a Enter Bypass Mode command). It uses the same sequence of cycles as the Quadruple Word Program command with the exception of the unlock cycles.

Block Lock Command. The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Three Bus Write cycles are required to issue the Block Lock command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block Lock command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Table 10 shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware reset or power-down/ power-up. They are cleared by a Blocks Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Unlock Command. The Blocks Unlock command is used to unlock a block, allowing the block to be programmed or erased.

Three Bus Write cycles are required to issue the Blocks Unlock command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block UnLock command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Table 10 shows the lock status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Lock-Down Command. A locked or unlocked block can be locked-down by issuing the Block Lock-Down command. A locked-down block cannot be programmed or erased, or have its protection status changed when $\overline{WPF}$ is Low, V_{IL}. When $\overline{WPF}$ is High, V_{IH}, the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Three Bus Write cycles are required to issue the Block Lock-Down command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block Lock-Down command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Locked-Down blocks revert to the locked (and not locked-down) state when the device is reset on power-down. Table 10 shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the device will return to Read Array mode. It is not necessary to pre-pro-

gram the block as the Program/Erase Controller does it automatically before erasing.

Six Bus Write cycles are required to issue the command.

- The first two write cycles unlock the Command Interface.
- The third write cycles sets up the command
- the fourth and fifth write cycles repeat the unlock sequence
- the sixth write cycle latches the block address and confirms the command.

Additional Block Erase confirm cycles can be issued to erase other blocks without further unlock cycles. All blocks must belong to the same bank; if a new block belonging to the other bank is given, the operation is aborted.

The additional Block Erase confirm cycles must be given within the DQ3 erase timeout period. Each time a new confirm cycle is issued the timeout period restarts. The status of the internal timer can be monitored through the level of DQ3, see Status Register section for more details.

Once the command is issued the device outputs the Status Register data when any address within the bank is read.

After the command has been issued the Flash Read/Reset command will be accepted during the DQ3 timeout period, after that only the Erase Suspend command will be accepted.

On successful completion of the Block Erase command, the device returns to Read Array mode.

Bank Erase Command. The Bank Erase command can be used to erase a bank. It sets all the bits within the selected bank to '1'. All previous data in the bank is lost. The Bank Erase command will ignore any protected blocks within the bank. If all blocks in the bank are protected then the Bank Erase operation will abort and the data in the bank will not be changed. It is not necessary to pre-program the bank as the Program/Erase Controller does it automatically before erasing.

As for the Block Erase command six Bus Write cycles are required to issue the command.

- The first two write cycles unlock the Command Interface.
- The third write cycles sets up the command
- the fourth and fifth write cycles repeat the unlock sequence
- the sixth write cycle latches the block address and confirms the command.

Once the command is issued the device outputs the Status Register data when any address within the bank is read.

On successful completion of the Bank Erase command, the device returns to Read Array mode.

Erase Suspend Command. The Erase Suspend command is used to pause a Block Erase operation. In a Dual Bank memory it can be used to read data within the bank where an Erase operation is in progress. It is also possible to program data in blocks not being erased.

One bus write cycle is required to issue the Erase Suspend command. The Program/Erase Controller suspends the Erase operation within 20µs of the Erase Suspend command being issued and bits 7, 6 and/ or 2 of the Status Register are set to '1'. The device is then automatically set to Read mode. The command can be addressed to any bank.

During Erase Suspend the memory will accept the Erase Resume, Program, Read CFI Query, Auto Select, Block Lock, Block Unlock and Block Lock-Down commands.

Erase Resume Command. The Erase Resume command can be used to restart the Program/ Erase Controller after an Erase Suspend command has paused it. One Bus Write cycle is required to issue the command. The command must be issued to an address within the bank being erased. The unlock cycles are not required.

Protection Register Program Command. The Protection Register Program command is used to Program the Protection Register (One-Time-Programmable (OTP) segment and Protection Register Lock). The OTP segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Four write cycles are required to issue the Protection Register Program command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Protection Register Program command.
- The fourth latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The OTP segment can be protected by programming bit 1 of the Protection Register Lock. The segment can be protected by programming bit 1 of the Protection Register Lock. Bit 1 of the Protection Register Lock also protects bit 2 of the Protection Register Lock. Programming bit 2 of the Protection Register Lock will result in a permanent protection of Parameter Block #0 (see Figure 5, Flash Security Block and Protection Register Memory Map). Attempting to program a previously

protected Protection Register will result in a Status Register error. The protection of the Protection Register and/or the Security Block is not reversible.

Table 4. Flash Commands

Commands	No of Cycles	Bus Operations													
		1st		2nd		3rd		4th		5th		6th		7th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset	1+	X	F0h	Read Memory Array until a new write cycle is initiated.											
	3+	555h	AAh	2AAh	55h	555h	F0h	Read Memory Array until a new write cycle is initiated.							
CFI Query	1+	55h	98h	Read CFI and Electronic Signature until a Read/Reset command is issued.											
Auto Select	3+	555h	AAh	2AAh	55h	555h	90h	Read Protection Register, Block Protection or Configuration Register Status until a Read/Reset command is issued.							
Set Configuration Register	4	555h	AAh	2AAh	55h	555h	60h	CRD	03h						
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	Read Data Polling or Toggle Bit until Program completes.					
Double Word Program	5	555h	AAh	2AAh	55h	555h	40h	PA1	PD1	PA2	PD2				
Quadruple Word Program	5	555h	AAh	2AAh	55h	555h	50h	PA1	PD1	PA2	PD2	PA3	PD3	PA4	PD4
Enter Bypass Mode	3	555h	AAh	2AAh	55h	555h	20h								
Exit Bypass Mode	2	X	90h	X	00h										
Program in Bypass Mode	2	X	A0h	PA	PD	Read Data Polling or Toggle Bit until Program completes.									
Double Word Program in Bypass Mode	3	X	40h	PA1	PD1	PA2	PD2								
Quadruple Word Program in Bypass Mode	3	X	50h	PA1	PD1	PA2	PD2	PA3	PD3	PA4	PD4				
Block Lock	4	555h	AAh	2AAh	55h	555h	60h	BA	01h						
Block Unlock	4	555h	AAh	2AAh	55h	555h	60h	BA	D0h						
Block Lock-Down	4	555h	AAh	2AAh	55h	555h	60h	BA	2Fh						
Block Erase	6+	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA	30h		
Bank Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA	10h		
Erase Suspend	1	X	B0h	Read until Toggle stops, then read all the data needed from any Blocks not being erased then Resume Erase.											
Erase Resume	1	BA	30h	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time											
Protection Register Program	4	555h	AAh	2AAh	55h	PA	C0h	PA	PD						

Note: X = Don't Care, BA = Block Address, PA = Program address, PD = Program Data, CRD = Configuration Register Data. For Coded cycles address inputs A12-A20 are don't care.

Table 5. Read Electronic Signature

Code	Device	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A7-A2	A8-A20	DQ15-DQ0
Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	X	0020h
Device Code	M36DR432AD	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	X	00A0h
	M36DR432BD	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	X	00A1h

Note: X = Don't care.

Table 6. Flash Read Block Protection

Block Status	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A20-A12	A7-A2	Other Addresses	DQ0	DQ1	DQ15-DQ2
Locked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	0	X	1	0	0000h
Unlocked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	0	X	0	0	0000h
Locked-Down Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	0	X	X	1	0000h

Note: X = Don't care.

Table 7. Configuration Register

$\overline{RPF}$ Function	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A7-A2	Other Addresses	DQ10	DQ9-DQ0 DQ15-DQ11
Reset	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	0	X	0	Don't Care
Reset/Power-Down	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	0	X	1	Don't Care

Note: X = Don't care.

Table 8. Read Protection Register

Word	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A20-A8	A7-0	DQ15-8	DQ7-3	DQ2	DQ1	DQ0
Lock	V_{IL}	V_{IL}	V_{IH}	X	80h	XXh	00000b	Security prot.data	OTP prot.data	0
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	X	81h	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	X	82h	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	X	83h	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	X	84h	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	X	85h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	X	86h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	X	87h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	X	88h	OTP data	OTP data	OTP data	OTP data	OTP data

Note: X= Don't care.

Table 9. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	M36DR432AD, M36DR432BD				Unit
	Min	Max	Typ	Typical after 100k W/E Cycles	
Parameter Block (4 KWord) Erase (Preprogrammed)		2.5	0.3	1	s
Main Block (32 KWord) Erase (Preprogrammed)		4	0.8	3	s
Bank Erase (Preprogrammed, Bank A)			3	6	s
Bank Erase (Preprogrammed, Bank B)			20	30	s
Chip Program (1)			20	25	s
Chip Program (Double Word, V_{PPF} = 12V) (1)			8		s
Word Program (2)		100	10		µs
Double Word Program (V_{PPF} = 12V)		100	8		µs
Quadruple Word Program (V_{PPF} = 12V)		100	8		µs
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. Excludes the time needed to execute the sequence for program command.
2. Same timing value if V_{PPF} = 12V

Flash Block Locking

The Flash memory features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has two levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.

The protection status of each block can be set to Locked, Unlocked, and Lock-Down. Table 10, defines all of the possible protection states ($\overline{WPF}$, DQ1, DQ0).

Reading a Block's Lock Status

The lock status of every block can be read in the Auto Select mode of the device. Subsequent reads at the address specified in Table 6, will output the protection status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when enter-

ing Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the locking system.

Locked State

The default status of all blocks on power-up or after a hardware reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will reset the device to Read Array mode. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

Unlocked State

Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state after a hardware reset or when the device is powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

Lock-Down State

Blocks that are Locked-Down (state (0,1,x))are protected from program and erase operations (as for Locked blocks) but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WPF}$ input pin. When $\overline{WPF}$=0 (V_{IL}), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WPF}$=1 (V_{IH}) the Lock-Down function is disabled (1,1,1) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-locked (1,1,1) and unlocked (1,1,0) as desired while $\overline{WPF}$ remains High. When $\overline{WPF}$ is Low, blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while $\overline{WPF}$ was High. Device reset or power-down resets all blocks, including those in Lock-Down, to the Locked state.

Locking Operations During Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Table 10. Flash Lock Status

Current Protection Status(1) (WPF, DQ1, DQ0)		Next Protection Status(1) (WPF, DQ1, DQ0)			
Current State	Program/Erase Allowed	After Block Lock Command	After Block Unlock Command	After Block Lock-Down Command	After WPF transition
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1(2)	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1(2)	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 (3)

Note: 1. The lock status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a locked block) as read in the Auto Select command with A1 = V_{IH} and A0 = V_{IL}.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to $\overline{WPF}$ status.
3. A $\overline{WPF}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

Flash Status Register

The Status Register provides information on the current or previous Program or Erase operations. Bus Read operations from any address within the bank, always read the Status Register during Program and Erase operations.

The various bits convey information about the status and any errors of the operation.

The bits in the Status Register are summarized in Table 12, Status Register Bits. Refer to Tables 11 and 12 in conjunction with the following text descriptions.

Data Polling Bit (DQ7). When Program operations are in progress, the Data Polling bit outputs the complement of the bit being programmed on DQ7. For a Double Word Program operation, it is the complement of DQ7 for the last Word written to the Command Interface.

During an Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing.

Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{WF}$ pulse for programming or after the sixth $\overline{WF}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. See Figure 22 for the Data Polling flowchart and Figure 13 for the Data Polling waveforms.

DQ7 will also flag an Erase Suspend by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During a program operation in Erase Suspend, DQ7 will have the same behavior as in the normal program.

Toggle Bit (DQ6). When Program or Erase operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following the toggling of either $\overline{GF}$ or $\overline{EF}$. The operation is completed when two successive reads give the same output data. The next read will output the bit last programmed or a '1' after erasing.

The Toggle Bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{WF}$ pulse for programming or after the sixth $\overline{WF}$ pulse for Erase. DQ6 will be set to '1' if a read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different from the block in Erase Suspend.

See Figure 16 for Toggle Bit flowchart and Figure 14 for Toggle Bit waveforms.

Toggle Bit (DQ2). Toggle Bit DQ2, together with DQ6, can be used to determine the device status during erase operations.

During Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will output data. DQ2 will be set to '1' during program operation and to '0' in erase operation. If a read operation is addressed to a block where an erase error has occurred, DQ2 will toggle.

Error Bit (DQ5). The Error Bit can be used to identify if an error occurs during a program or erase operation.

The Error Bit is set to ‘1’ when a program or erase operation has failed. When it is set to ‘0’ the program or erase operation was successful.

If any Program command is used to try to set a bit from ‘0’ to ‘1’ Status Register Error bit DQ5 will be set to ‘1’, only if V_{PP} is in the range of 11.4V to 12.6V.

The Error Bit is reset by a Read/Reset command.

Erase Timer Bit (DQ3). The Erase Timer bit is used to indicate the timeout period for an erase operation.

When the last block Erase command has been entered to the Command Interface and it is waiting for the erase operation to start, the Erase Timer Bit is set to ‘0’. When the erase timeout period is finished, DQ3 returns to ‘1’, (80µs to 120µs).

DQ0, DQ1 and DQ4 are reserved for future use and should be masked.

Table 11. Polling and Toggle Bits

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	N/A
Erase Suspend Read (in Erase Suspend block)	1	1	Toggle
Erase Suspend Read (outside Erase Suspend block)	DQ7	DQ6	DQ2
Erase Suspend Program	$\overline{DQ7}$	Toggle	1

Table 12. Status Register Bits

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase complete or erase block in Erase Suspend.	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase success.
		'0'	Erase in progress	
		DQ	Program complete or data of non erase block during Erase Suspend.	
		$\overline{DQ}$	Program in progress(2)	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program in progress	Successive reads output complementary data on DQ6 while Programming or Erase operations are in progress. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program complete	
		'-1-1-1-1-1-1-1-'	Erase complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase in progress	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend
		'0'	Erase Timeout Period in progress	An additional block to be erased in parallel can be entered to the P/E.C provided that it belongs to the same bank
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase Suspend read in the Erase Suspended Block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block.
		1	Program in progress or Erase complete.	
		DQ	Erase Suspend read on non Erase Suspend block.	
1	Reserved			
0	Reserved			

Note: 1. Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive read operations.
2. In case of double word program $\overline{DQ7}$ refers to the last word input.

SRAM COMPONENT

The SRAM is a 4 Mbit (256Kb x16) low-power consumption memory array with low V_{DDS} data retention.

SRAM Operations

The following operations can be performed using the appropriate bus cycles: Read Array, Write Array, Output Disable, Power Down (see Table 2).

Read. Read operations are used to output the contents of the SRAM Array. The SRAM is in Read mode whenever Write Enable ($\overline{WS}$) is at V_{IH} with Output Enable ($\overline{GS}$) at V_{IL}, Chip Enable $\overline{ES}$ and $\overline{UBS}$, $\overline{LBS}$ combinations are asserted.

Valid data will be available at the output pins within t_{AVQV} after the last stable address, provided that $\overline{GS}$ is Low and $\overline{ES}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV} (see Table 23, Figures 17 and 18).

Write. Write operations are used to write data in the SRAM. The SRAM is in Write mode whenever the $\overline{WS}$ and $\overline{ES}$ pins are at V_{IL}. Either the Chip Enable input ($\overline{ES}$) or the Write Enable input ($\overline{WS}$) must be de-asserted during address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active and $\overline{WS}$ at V_{IL}. A Write begins at the latest transition among $\overline{ES}$ going to V_{IL} and $\overline{WS}$ going to V_{IL}. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the rising edge of $\overline{ES}$ or the rising edge of $\overline{WS}$, whichever occurs first.

If the Output is enabled ($\overline{ES}$=V_{IL} and $\overline{GS}$=V_{IL}), then $\overline{WS}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{ES}$, whichever occurs first, and remain valid for t_{WHDX} and t_{EHAX} (see Table 24, Figure 20, 22, 24).

Standby/Power-Down. The SRAM chip has a Chip Enable power-down feature which invokes an automatic standby mode (see Table 23, Figure 19) whenever either Chip Enable is de-asserted ($\overline{ES}$=V_{IH}).

Data Retention. The SRAM data retention performances as V_{DDS} go down to V_{DR} are described in Table 25 and Figure 24. In $\overline{ES}$ controlled data retention mode, minimum standby current mode is entered when $\overline{ES} \geq V_{DDS} - 0.2V$.

Output Disable. The data outputs are high impedance when the Output Enable ($\overline{GS}$) is at V_{IH} with Write Enable ($\overline{WS}$) at V_{IH}.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 13. Absolute Maximum Ratings(1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{DD}(3)+0.5	V
V_{DDF}	Supply Voltage	–0.5 to 2.7	V
V_{DDS}	SRAM Chip Supply Voltage	–0.5 to 2.4	V
V_{PPF}	Program Voltage	–0.5 to 13	V

Note: 1. Minimum voltage may undershoot to –2V during transition and for less than 20ns.
2. Depends on range.
3. $V_{DD} = V_{DDS} = V_{DDF}$.

DC AND AC PARAMETERS

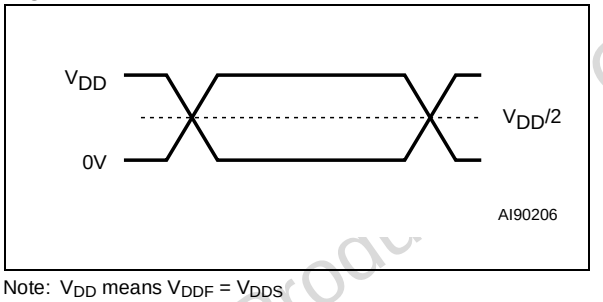
This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 14, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 14. Operating and AC Measurement Conditions

Parameter	SRAM		Flash				Units
	70		85		100, 120		
	Min	Max	Min	Max	Min	Max	
V_{DDF} Supply Voltage	-	-	1.8	2.2	1.65	2.2	V
V_{DDS} Supply Voltage	1.65	2.2	-	-	-	-	V
V_{PPF} Supply Voltage			11.4	12.6	11.4	12.6	V
Ambient Operating Temperature	– 40	85	– 40	85	– 40	85	°C
Load Capacitance (C_L)	30	5	30		30		pF
Input Rise and Fall Times		2		4		4	ns
Input Pulse Voltages(1)	0 to V_{DD}		0 to V_{DD}		0 to V_{DD}		V
Input and Output Timing Ref. Voltages(1)	$V_{DD}/2$		$V_{DD}/2$		$V_{DD}/2$		V

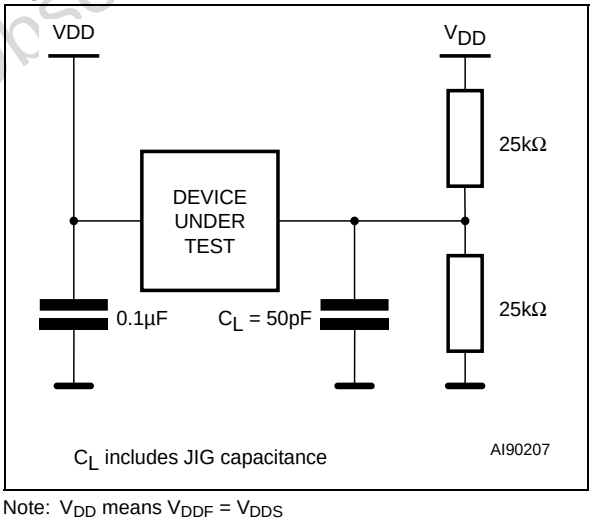
Note: 1. $V_{DD} = V_{DDS} = V_{DDF}$

Figure 6. AC Measurement I/O Waveform



Note: V_{DD} means $V_{DDF} = V_{DDS}$

Figure 7. AC Measurement Load Circuit



Note: V_{DD} means $V_{DDF} = V_{DDS}$

Table 15. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		15	pF

Note: Sampled only, not 100% tested.

Table 16. Flash DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DD}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DD}$			±5	µA
I_{CC1}	Supply Current (Read Mode)	$\overline{EF} = V_{IL}$, $\overline{GF} = V_{IH}$, f = 6MHz		3	6	mA
I_{CC2}	Supply Current (Power-Down)	$\overline{RPF} = V_{SS} \pm 0.2V$		2	10	µA
I_{CC3}	Supply Current (Standby)	$\overline{EF} = V_{DD} \pm 0.2V$		10	50	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Word Program, Block Erase in progress		10	20	mA
I_{CC5} (1)	Supply Current (Dual Bank)	Program/Erase in progress in one Bank, Read in the other Bank		13	26	mA
I_{PPF1}	V_{PPF} Supply Current (Program or Erase)	$V_{PPF} = 12V \pm 0.6V$		2	5	mA
I_{PPF2}	V_{PPF} Supply Current (Standby or Read)	$V_{PPF} \le V_{DD}$		0.2	5	µA
		$V_{PPF} = 12V \pm 0.6V$		100	400	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		$V_{DD} – 0.4$		$V_{DD} + 0.4$	V
V_{OL}	Output Low Voltage	$I_{OL} = 100µA$			0.1	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = –100µA$	$V_{DD} –0.1$			V
V_{PPF}(2,3)	V_{PPF} Supply Voltage (Program or Erase)		–0.4		$V_{DD} + 0.4$	V
		Double Word Program	11.4		12.6	V

Note: 1. Sampled only, not 100% tested.
2. V_{PPF} may be connected to 12V power supply for a total of less than 100 hrs.
3. For standard program/erase operation V_{PPF} is don't care.

Table 17. SRAM DC Characteristics
(T_A = –40 to 85°C; V_{DDF} = V_{DDS} = 1.65V to 2.2V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{OZ}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDS}$, output disabled	-1	+1	+1	µA
I_{IX}	Input Load Current	$0V \le V_{IN} \le V_{DDS}$	-1	±1	+1	µA
I_{DDS}	V_{DD} Standby Current	$\overline{ES} \ge V_{DDS} - 0.2V$, $V_{IN} \ge V_{DDS} - 0.2V$ or $V_{IN} \le 0.2V$, f=0 V_{DDS} = 2.2V		1	10	µA
I_{DD}	Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS levels V_{DDS} = 2.2V		4	7	mA
		I_{OUT} = 0 mA, f = 0Hz CMOS levels		1	5	mA
V_{IL}	Input Low Voltage	V_{DDS} = 1.65V	–0.5		0.4	V
V_{IH}	Input High Voltage	V_{DDS} = 2.2V	1.4		V_{DDS} +0.2V	V
V_{OL}	Output Low Voltage	V_{DDS} = 1.65V I_{OL} = 0.1µA			0.2	V
V_{OH}	Output High Voltage	V_{DDS} = 1.65V I_{OH} = –0.1µA	1.4			V

Note: 1. I_{DDES} and I_{DDWS} are specified with device deselected. If device is read while in erase suspend, current draw is sum of I_{DDES} and I_{DDR}. If the device is read while in program suspend, current draw is the sum of I_{DDWS} and I_{DDR}.
2. V_{IN} = V_{IL} or V_{IH}

Figure 8. Flash Random Read AC Waveforms

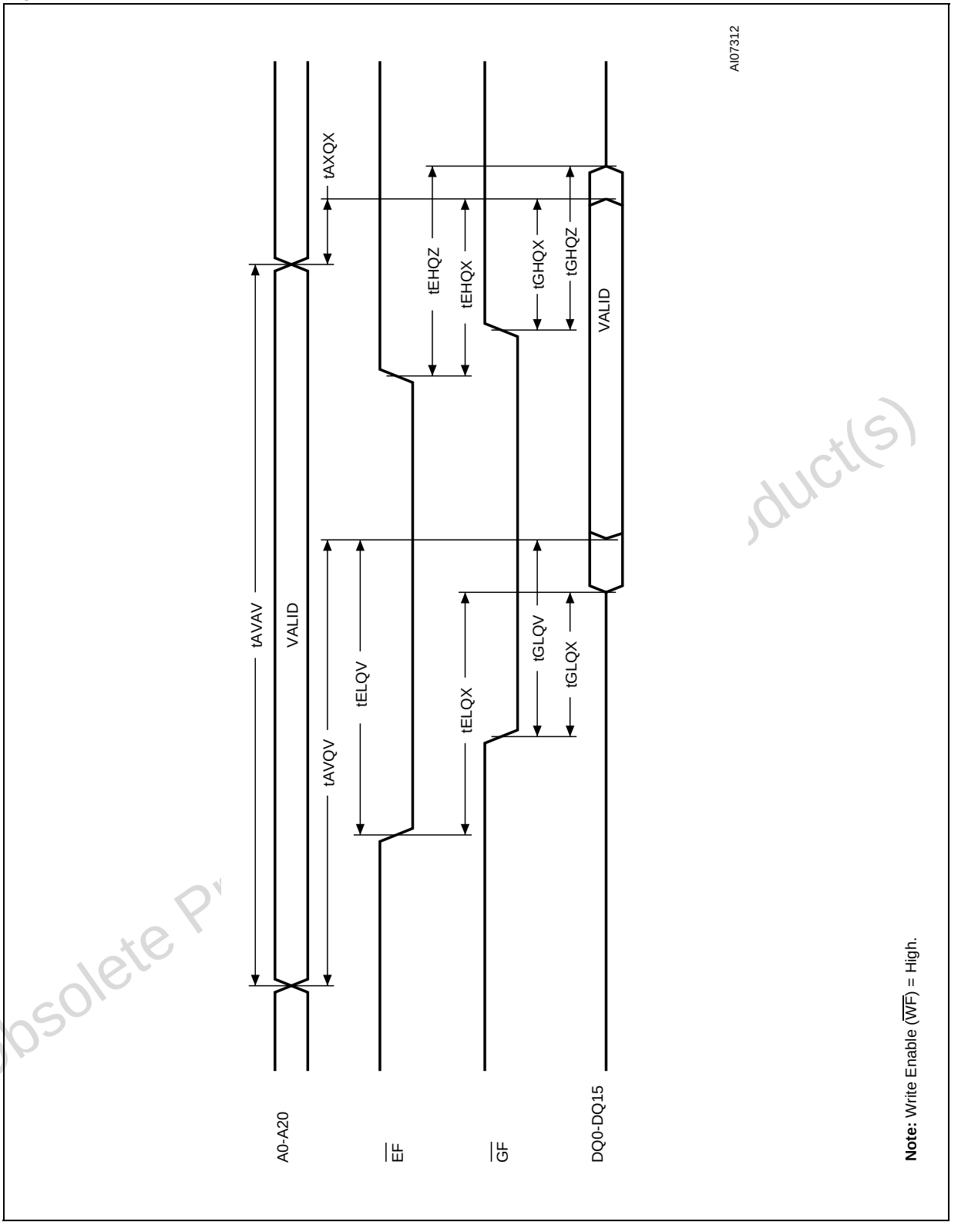


Figure 9. Flash Page Read AC Waveforms

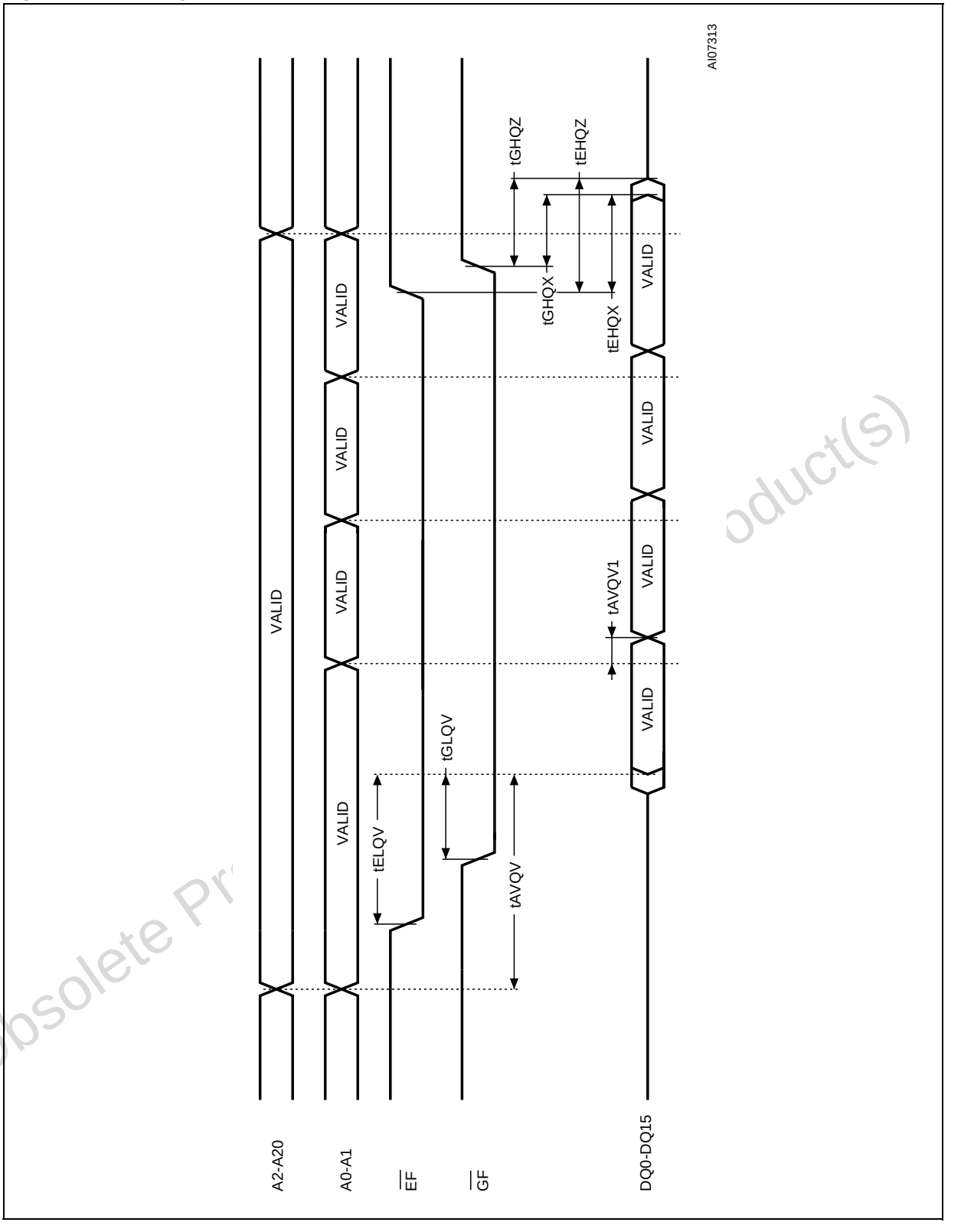
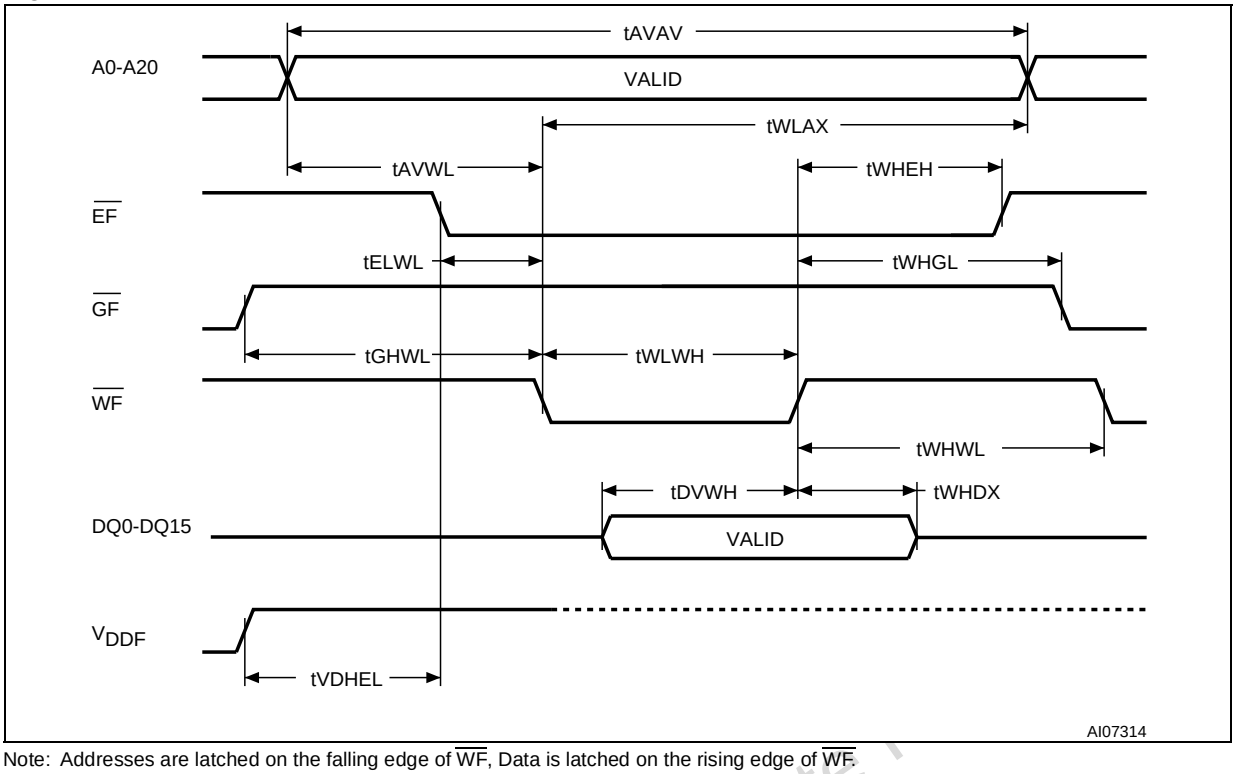


Table 18. Flash Read AC Characteristics

Symbol	Alt	Parameter	Test Condition	M36DR432AD, M36DR432BD						Unit
				85		100		120		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}	85(3)		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}		85(3)		100		120	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}		30(3)		35		45	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{GF}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{GF}$ = V_{IL}		85(3)		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{EF}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{EF}$ = V_{IL}		25(3)		25		35	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{GF}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{GF}$ = V_{IL}		20(3)		25		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{EF}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{EF}$ = V_{IL}		20(3)		25		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{GF}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EF}$ without increasing t_{ELQV}.
3. To be characterized.

Figure 10. Flash Write AC Waveforms, Write Enable Controlled



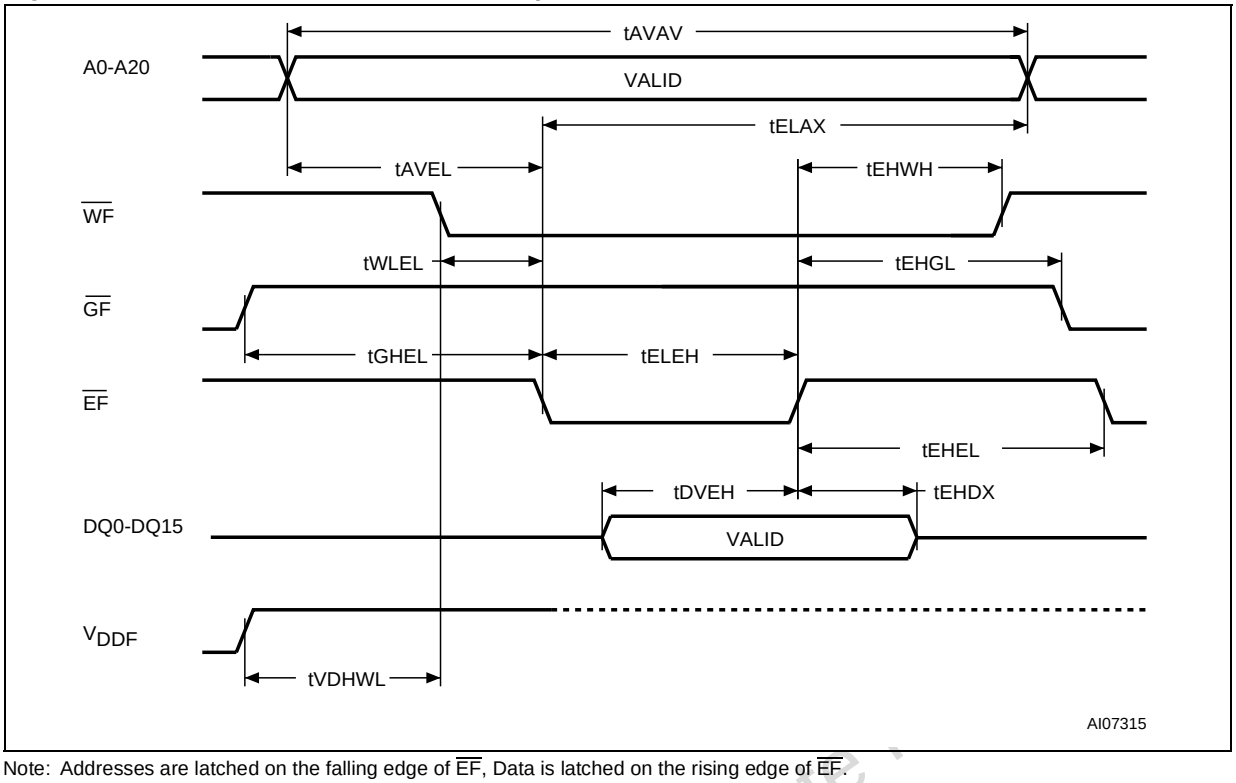
Note: Addresses are latched on the falling edge of $\overline{WF}$, Data is latched on the rising edge of $\overline{WF}$.

Table 19. Flash Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter	M36DR432AD, M36DR432BD						Unit
			85		100		120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	85(1)		100		120		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50(1)		50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40(1)		50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		30		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		ns
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	30		30		30		ns
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete During Program/Erase		15		15		15	µs

Note: 1. To be characterized.

Figure 11. Flash Write AC Waveforms, Chip Enable Controlled



Note: Addresses are latched on the falling edge of $\overline{EF}$, Data is latched on the rising edge of $\overline{EF}$.

Table 20. Flash Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter	M36DR432AD, M36DR432BD						Unit
			85		100		120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	85(1)		100		120		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50(1)		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40(1)		50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		30		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		0		ns
t_{VDHWL}	t_{VCS}	V_{DD} High to Write Enable Low	50		50		50		µs
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	30		30		30		ns
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete During Program/Erase		15		15		15	µs

Note: 1. To be characterized

Figure 12. Flash Reset/Power-Down AC Waveform

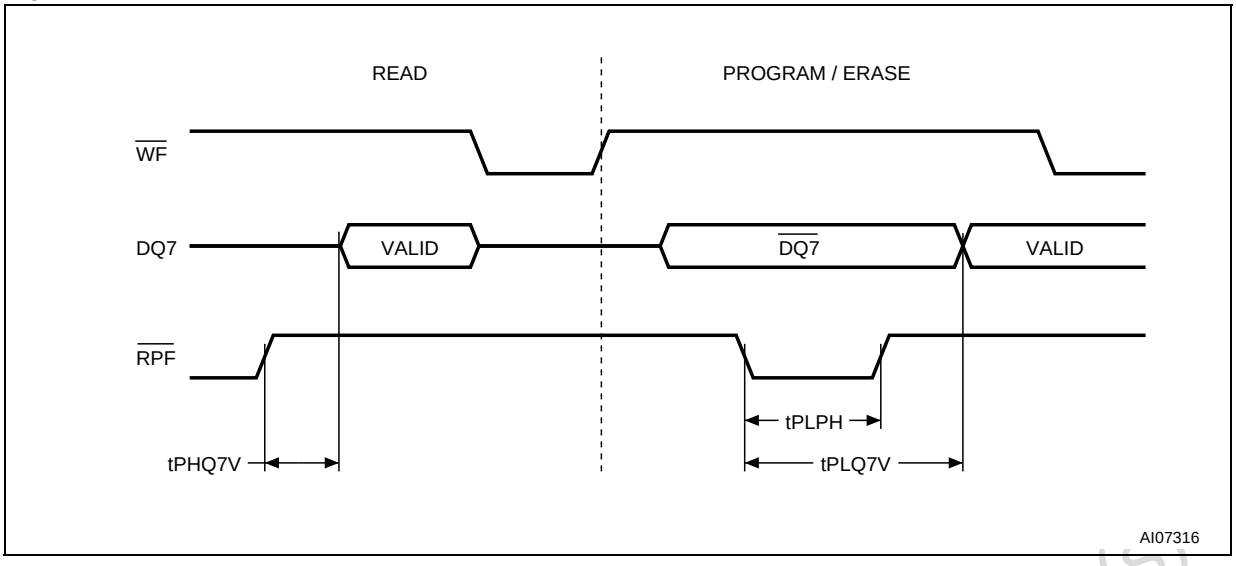


Table 21. Flash Reset/Power-Down AC Characteristics

Symbol	Alt	Parameter	Test Condition	M36DR432AD, M36DR432BD						Unit
				85		100		120		
				Min	Max	Min	Max	Min	Max	
t_{PHQ7V1}		$\overline{RPF}$ High to Data Valid (Read Mode)			150		150		150	ns
t_{PHQ7V2}		$\overline{RPF}$ High to Data Valid (Reset/Power-Down enabled)			50		50		50	µs
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete	During Program		10		10		10	µs
			During Erase		20		20		20	µs
t_{PLPH}	t_{RP}	$\overline{RPF}$ Pulse Width		50		50		50		ns

Figure 13. Flash Data Polling DQ7 AC Waveforms

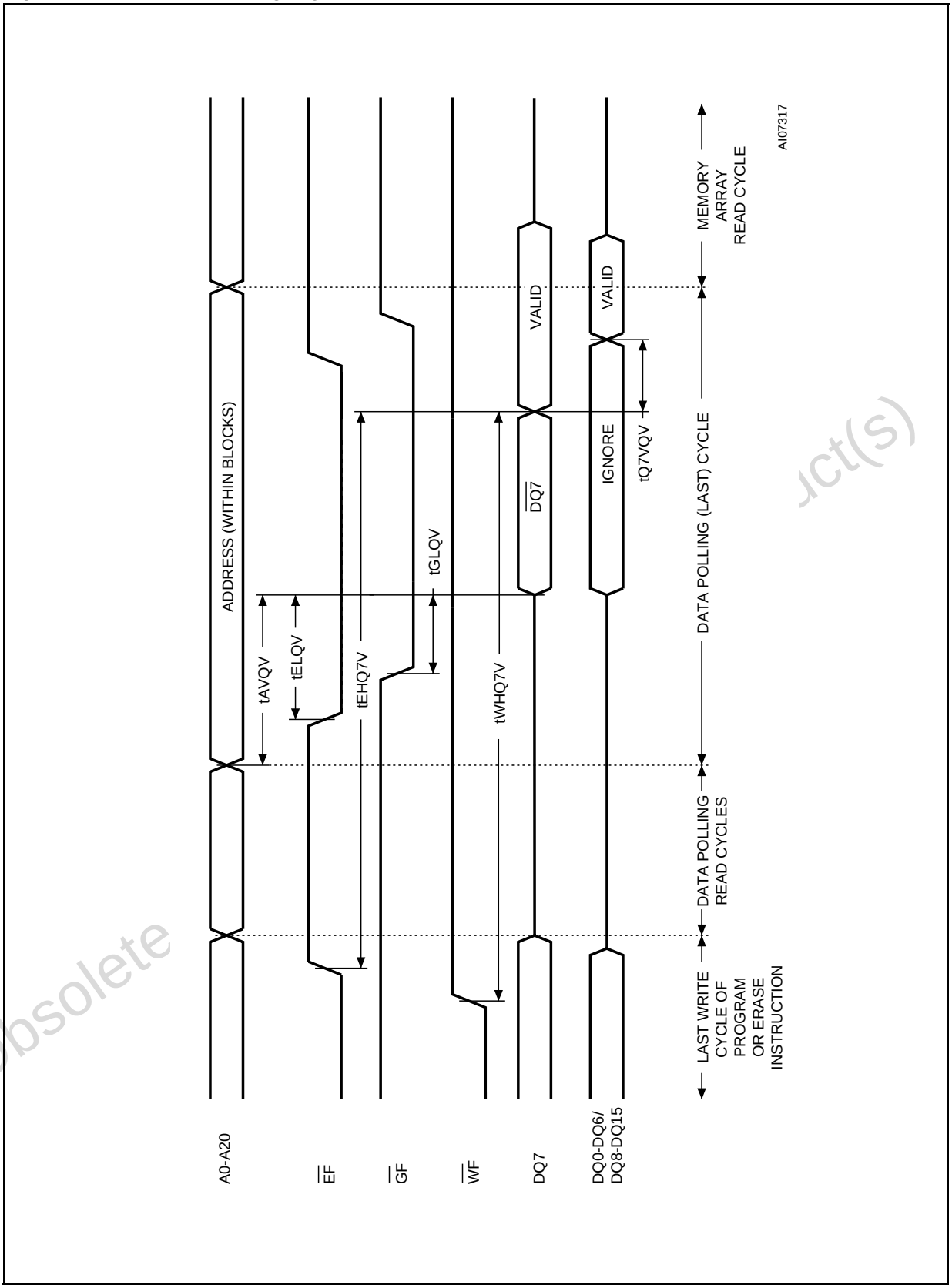
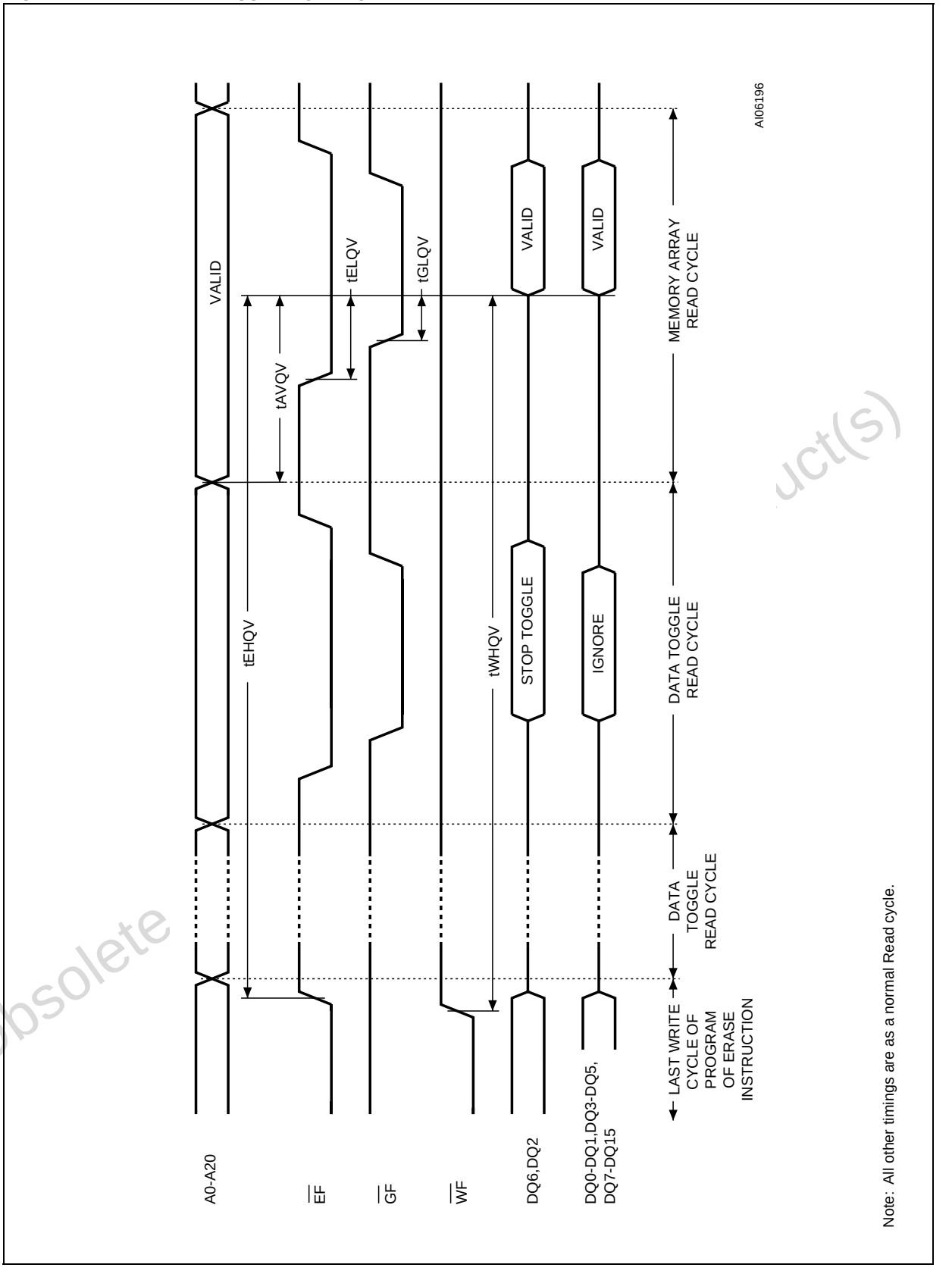


Figure 14. Flash Data Toggle DQ6, DQ2 AC Waveforms



Note: All other timings are as a normal Read cycle.

Table 22. Flash Data Polling and Toggle Bits AC Characteristics

Symbol	Parameter	M36DR432AD, M36DR432BD		Unit
		Min	Max	
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, $\overline{WF}$ Controlled)	8	100	µs
	Write Enable High to DQ7 Valid (Block Erase, $\overline{WF}$ Controlled)	0.8	4	s
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, $\overline{EF}$ Controlled)	8	100	µs
	Chip Enable High to DQ7 Valid (Block Erase, $\overline{EF}$ Controlled)	0.8	4	s
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		0	ns
t_{WHQV}	Write Enable High to Output Valid (Program)	8	100	µs
	Write Enable High to Output Valid (Block Erase)	0.8	4	s
t_{EHQV}	Chip Enable High to Output Valid (Program)	8	100	µs
	Chip Enable High to Output Valid (Block Erase)	0.8	4	s

Note: All other timings are defined in Read AC Characteristics

Figure 15. Flash Data Polling Flowchart

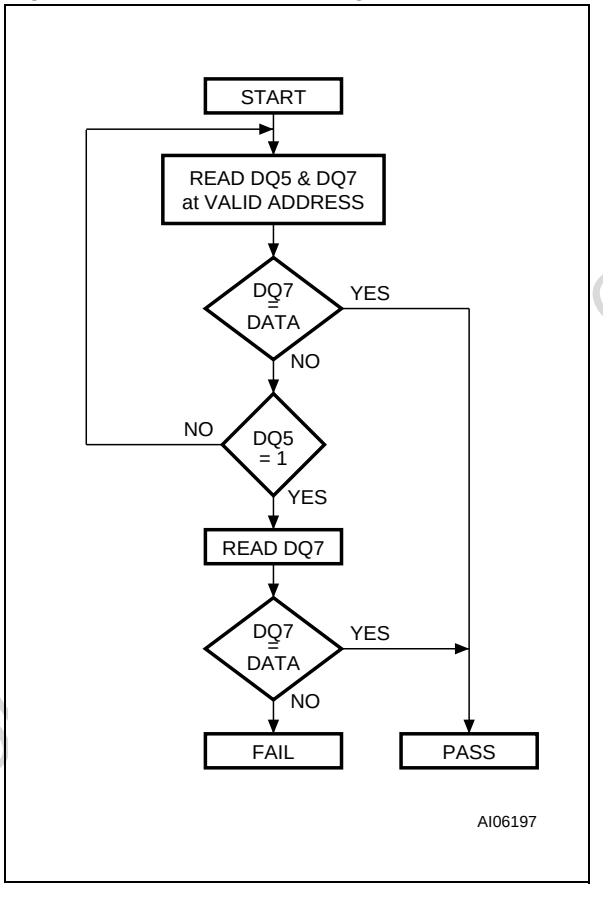


Figure 16. Flash Data Toggle Flowchart

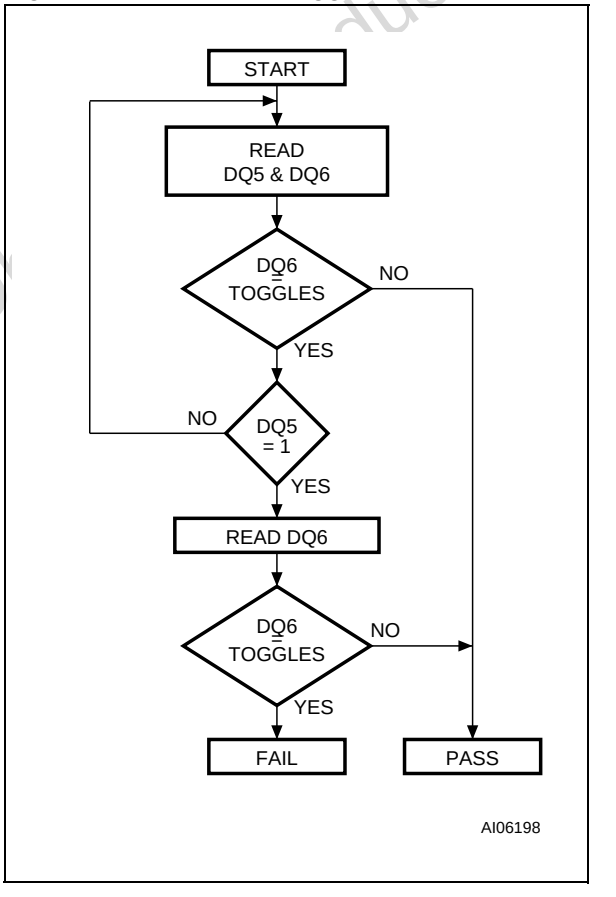
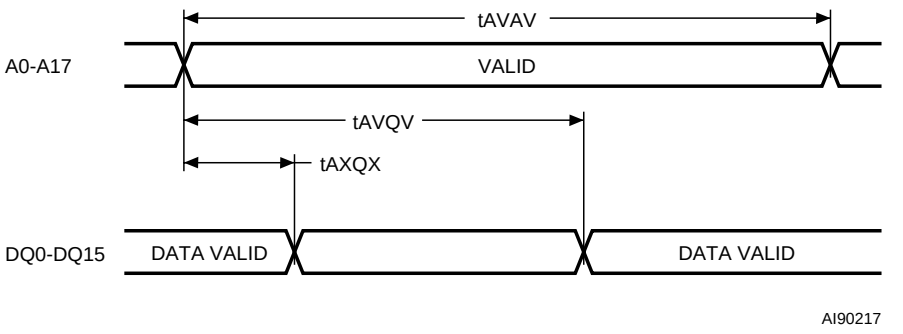
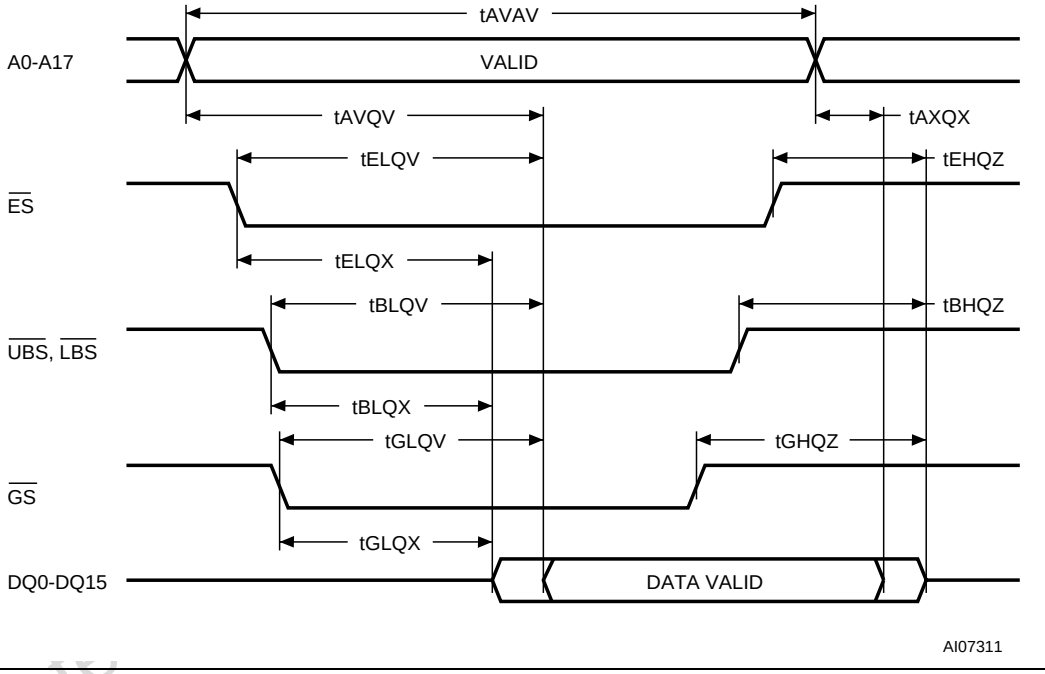


Figure 17. SRAM Read Mode AC Waveforms, Address Controlled with $\overline{UBS}$ = $\overline{LBS}$ = V_{IL}



Note: $\overline{ES}$ = Low, $\overline{GS}$ = Low, $\overline{WS}$ = High.

Figure 18. SRAM Read AC Waveforms, $\overline{ES}$ or $\overline{GS}$ Controlled



Note: Write Enable ($\overline{WS}$) = High.

Figure 19. SRAM Standby AC Waveforms

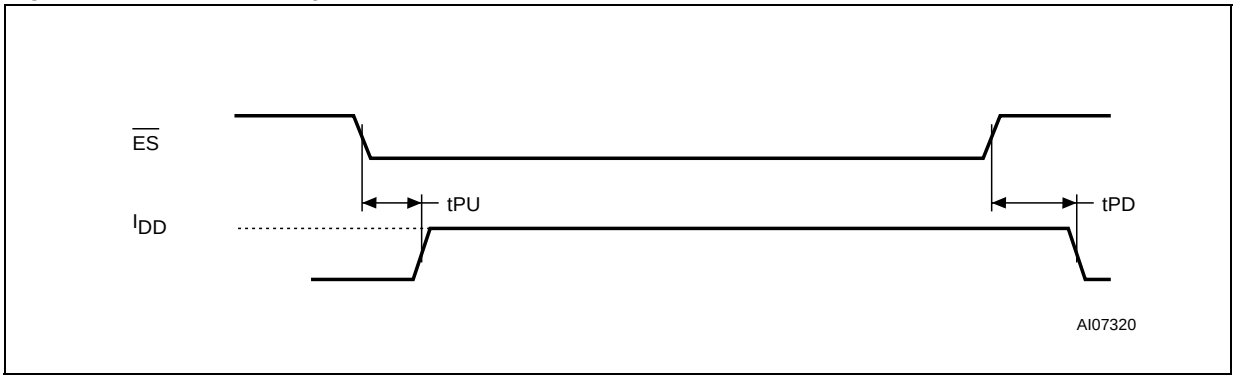
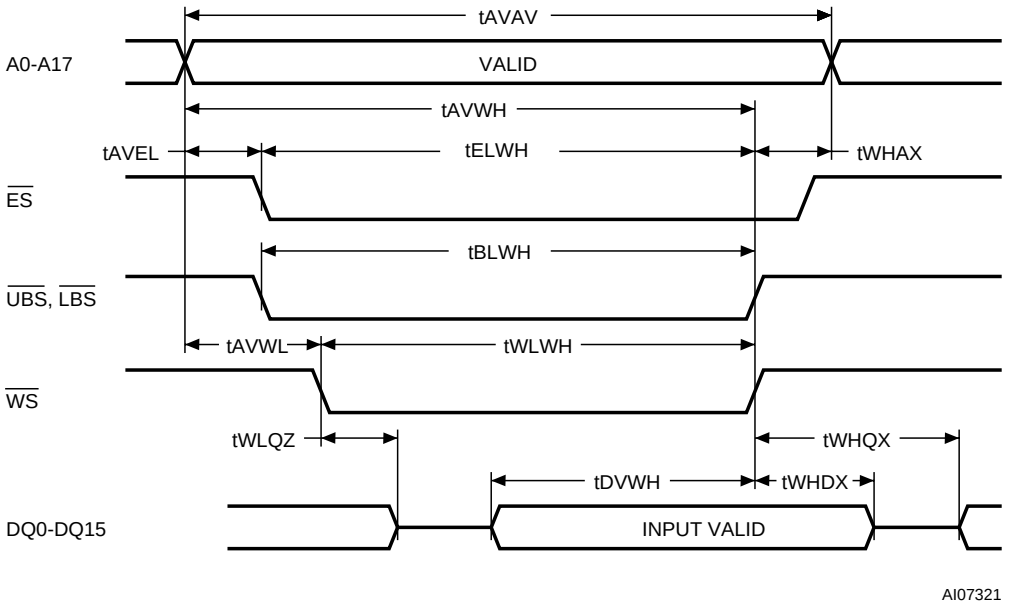


Table 23. SRAM Read AC Characteristics)

Symbol	Alt	Parameter	SRAM		Unit
			70		
			Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	70		ns
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	10		ns
t_{BHQZ}	t_{BHZ}	$\overline{UBS}$, $\overline{LBS}$ Disable to Hi-Z Output		25	ns
t_{BLQV}	t_{BA}	$\overline{UBS}$, $\overline{LBS}$ Access Time		45	ns
t_{BLQX}	t_{BLZ}	$\overline{UBS}$, $\overline{LBS}$ Enable to Low-Z Output	5		ns
t_{EHQZ}	t_{HZ}	Chip Enable High to Output Hi-Z		25	ns
t_{ELQV}	t_{ACE}	Chip Enable Low to Output Valid		70	ns
t_{ELQX}	t_{LZ}	Chip Enable Low to Output Transition	5		ns
t_{GHQZ}	t_{OHZ}	Output Enable High to Output Hi-Z		25	ns
t_{GLQV}	t_{EO}	Output Enable Low to Output Valid		35	ns
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition	5		ns
t_{PD} (1)		Chip Enable High to Power Down		70	ns
t_{PU} (1)		Chip Enable Low to Power Up	0		ns

Note: 1. Sampled only. Not 100% tested.

Figure 20. SRAM Write AC Waveforms, $\overline{WS}$ Controlled with $\overline{GS}$ Low



Note: Output Enable ($\overline{GS}$) = Low.

Figure 21. SRAM Write AC Waveforms, $\overline{WS}$ Controlled with $\overline{GS}$ High

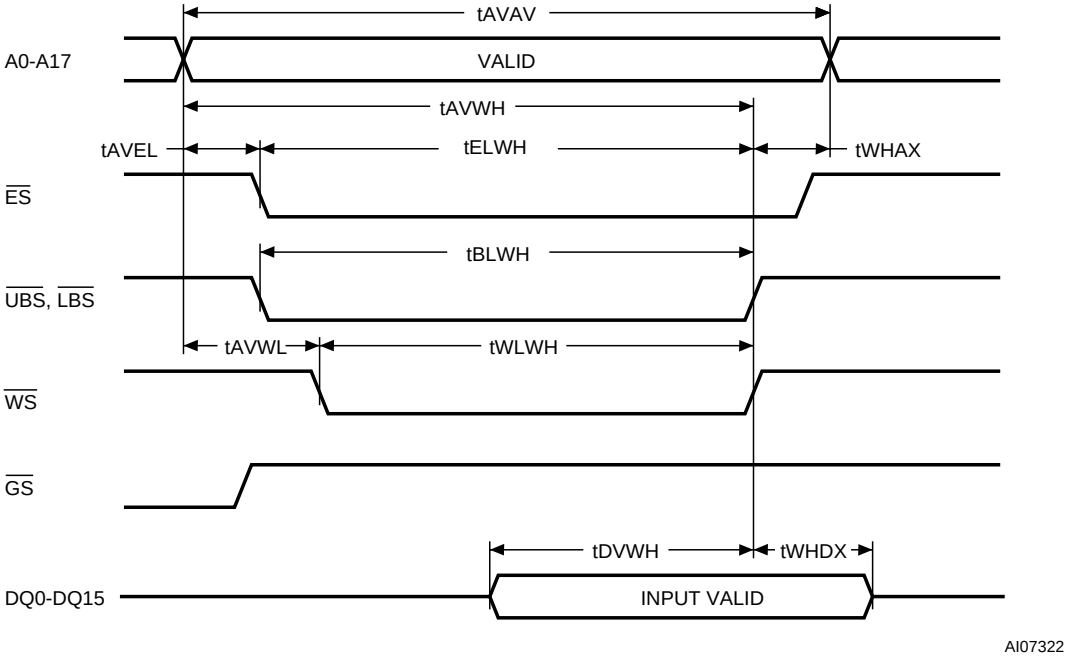


Figure 22. SRAM Write Cycle Waveform, $\overline{UBS}$ and $\overline{LBS}$ Controlled, $\overline{G}$ Low

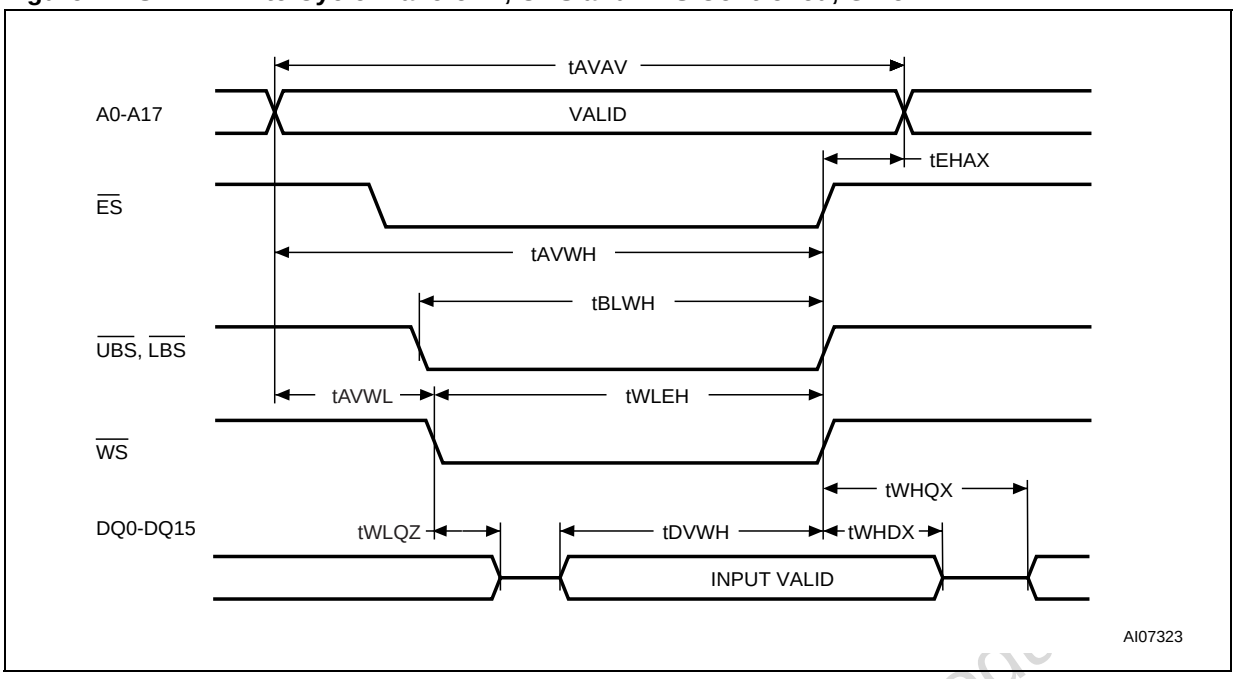
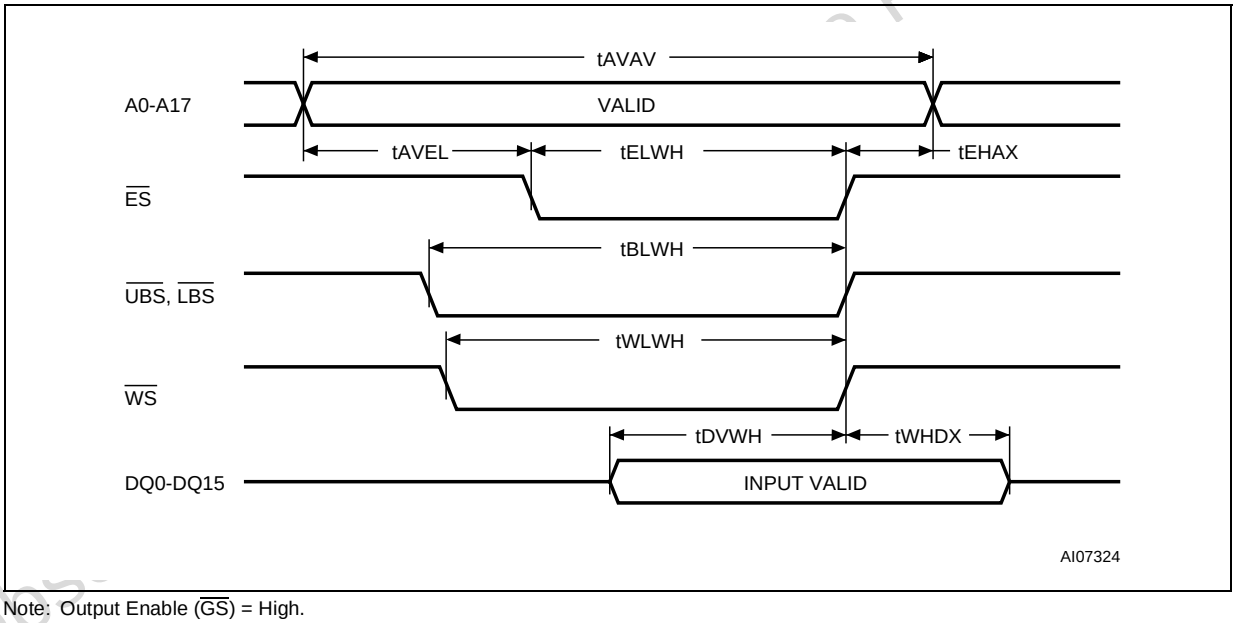


Figure 23. SRAM Write AC Waveforms, $\overline{ES}$ Controlled



Note: Output Enable ($\overline{GS}$) = High.

Table 24. SRAM Write AC Characteristics

Symbol	Alt	Parameter	SRAM		Unit
			70		
			Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		ns
t_{AVEL}	t_{AS} (1)	Address Valid to Chip Enable Low	0		ns
t_{AVWH}	t_{AW}	Address Valid to Write Enable High	60		ns
t_{AVWL}	t_{AS} (1)	Address Valid to Write Enable Low	0		ns
t_{BLWH}	t_{BW}	$\overline{UBS}$, $\overline{LBS}$ Valid to End of Write		60	ns
t_{DVWH}	t_{DW}	Input Valid to Write Enable High	30		ns
t_{EHAX}	t_{WR} (2)	Chip Enable High to Address Transition	0		ns
t_{ELWH},	t_{CW} (3)	Chip Select to End of Write	60		ns
t_{WHAX}	t_{WR} (2)	Write Enable High to Address Transition	0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{WHQX}	t_{OW}	Write Enable High to Output Transition	10		ns
t_{WLQZ}	t_{WHZ}	Write Enable Low to Output Hi-Z		25	ns
t_{WLWH}	t_{WP} (4)	Write Enable Pulse Width	50		ns

Note: 1. t_{AS} is measured from the address valid to the beginning of write.
2. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{ES}$ or $\overline{WS}$ goes High.
3. t_{CW} is measured from $\overline{ES}$ going Low end of write.
4. A Write occurs during the overlap (t_{WP}) of Low $\overline{ES}$ and Low $\overline{WS}$. A write begins when $\overline{ES}$ goes Low and $\overline{WS}$ goes Low with asserting $\overline{UBS}$ or $\overline{LBS}$ for single byte operation or simultaneously asserting $\overline{UBS}$ and $\overline{LBS}$ for double byte operation. A write ends at the earliest transition when $\overline{ES}$ goes High and $\overline{WS}$ goes High. The t_{WP} is measured from the beginning of write to the end of write.

Figure 24. SRAM Low V_{DDS} Data Retention AC Waveforms, $\overline{ES}$ Controlled

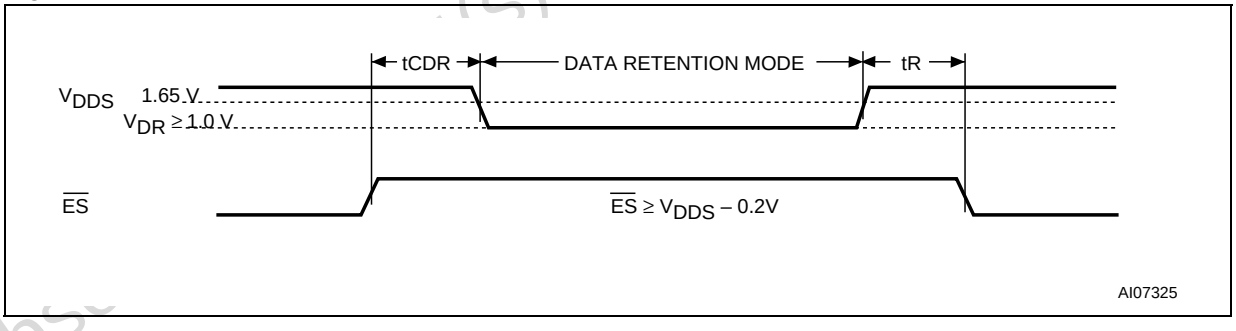


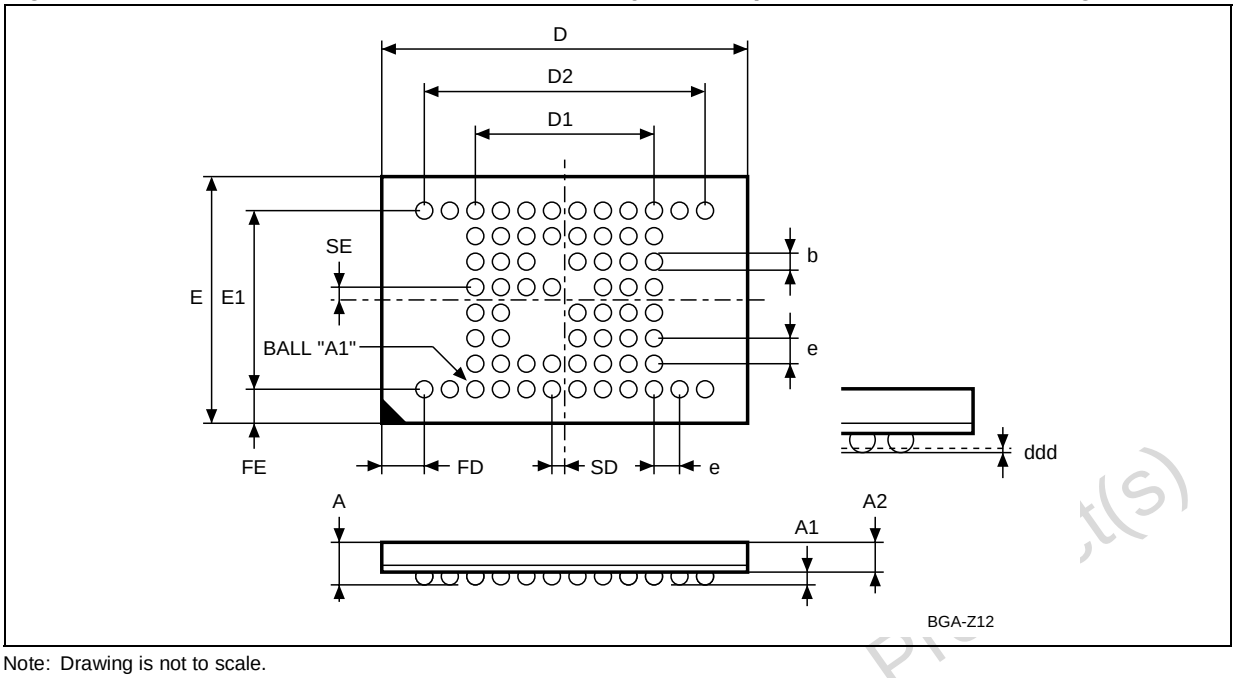
Table 25. SRAM Low V_{DDS} Data Retention Characteristics (1, 2)

Symbol	Parameter	Test Condition	Min	Typical	Max	Unit
I_{DDDR}	Supply Current (Data Retention)	V_{DDS} = 1.0V, $\overline{ES} \geq V_{DDS} - 0.2V$ no input may exceed V_{DDS} + 2V		0.5	10	µA
V_{DR}	Supply Voltage (Data Retention)	$\overline{ES} \geq V_{DDS} - 0.2V$	1		2.2	V
t_{CDR}	Chip Disable to Data Retention Time	$\overline{ES} \geq V_{DDS} - 0.2V$	0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Note: 1. All other Inputs $V_{IH} \leq V_{DDS} - 0.2V$ or $V_{IL} \leq 0.2V$.
2. Sampled only. Not 100% tested.

PACKAGE MECHANICAL

Figure 25. Stacked LFBGA 12x8mm - 8x8 ball array, 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 26. Stacked LFBGA 12x8mm - 8x8 ball array, 0.8mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.250			0.0098	
A2			1.100			0.0433
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	12.000	–	–	0.4724	–	–
D1	5.600	–	–	0.2205	–	–
D2	8.800	–	–	0.3465	–	–
ddd			0.100			0.0039
E	8.000	–	–	0.3150	–	–
E1	5.600	–	–	0.2205	–	–
e	0.800	–	–	0.0315	–	–
FD	1.600	–	–	0.0630	–	–
FE	1.200	–	–	0.0472	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

PART NUMBERING

Table 27. Ordering Information Scheme

Example: M36 D R 4 32A D 10 ZA 6 T

Device Type
M36 = MMP (Flash + SRAM)

Architecture
D = Dual Bank, Page Mode

Operating Voltage
R = V_{DDF} = V_{DDS} = 1.65V to 2.2V

SRAM Chip Size & Organization
4 = 4 Mbit (256Kb x 16 bit)

Flash Specification Details
32A = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Top Configuration
32B = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Bottom Configuration

SRAM Specification Details
D = Asynchronous SRAM, 0.16µm, 70ns speed

Speed
85 = 85ns (to be characterized)
10 = 100ns
12 = 120ns

Package
ZA = LFBGA66: 0.8mm pitch

Temperature Range
6 = –40 to 85°C

Option
T = Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESSES

Table 28. Bank A, Top Boot Block Addresses M36DR432AD

#	Size (KWord)	Address Range
14	4	1FF000h-1FFFFFh
13	4	1FE000h-1FEFFFh
12	4	1FD000h-1FDFFFh
11	4	1FC000h-1FCFFFh
10	4	1FB000h-1FBFFFh
9	4	1FA000h-1FAFFFh
8	4	1F9000h-1F9FFFh
7	4	1F8000h-1F8FFFh
6	32	1F0000h-1F7FFFh
5	32	1E8000h-1EFFFFh
4	32	1E0000h-1E7FFFh
3	32	1D8000h-1DFFFFh
2	32	1D0000h-1D7FFFh
1	32	1C8000h-1CFFFFh
0	32	1C0000h-1C7FFFh

Table 29. Bank B, Top Boot Block Addresses M36DR432AD

#	Size (KWord)	Address Range
55	32	1B8000h-1BFFFFh
54	32	1B0000h-1B7FFFh
53	32	1A8000h-1AFFFFh
52	32	1A0000h-1A7FFFh
51	32	198000h-19FFFFh
50	32	190000h-197FFFh
49	32	188000h-18FFFFh
48	32	180000h-187FFFh
47	32	178000h-17FFFFh
46	32	170000h-177FFFh
45	32	168000h-16FFFFh
44	32	160000h-167FFFh
43	32	158000h-15FFFFh
42	32	150000h-157FFFh
41	32	148000h-14FFFFh
40	32	140000h-147FFFh
39	32	138000h-13FFFFh
38	32	130000h-137FFFh
37	32	128000h-12FFFFh
36	32	120000h-127FFFh
35	32	118000h-11FFFFh
34	32	110000h-117FFFh
33	32	108000h-10FFFFh
32	32	100000h-107FFFh
31	32	0F8000h-0FFFFFh
30	32	0F0000h-0F7FFFh
29	32	0E8000h-0EFFFFh
28	32	0E0000h-0E7FFFh
27	32	0D8000h-0DFFFFh
26	32	0D0000h-0D7FFFh
25	32	0C8000h-0CFFFFh
24	32	0C0000h-0C7FFFh
23	32	0B8000h-0BFFFFh
22	32	0B0000h-0B7FFFh
21	32	0A8000h-0AFFFFh
20	32	0A0000h-0A7FFFh
19	32	098000h-09FFFFh
18	32	090000h-097FFFh
17	32	088000h-08FFFFh
16	32	080000h-087FFFh
15	32	078000h-07FFFFh
14	32	070000h-077FFFh
13	32	068000h-06FFFFh
12	32	060000h-067FFFh
11	32	058000h-05FFFFh
10	32	050000h-057FFFh
9	32	048000h-04FFFFh
8	32	040000h-047FFFh
7	32	038000h-03FFFFh
6	32	030000h-037FFFh
5	32	028000h-02FFFFh
4	32	020000h-027FFFh
3	32	018000h-01FFFFh
2	32	010000h-017FFFh
1	32	008000h-00FFFFh
0	32	000000h-007FFFh

Table 30. Bank B, Bottom Boot Block Addresses M36DR432BD

#	Size (KWord)	Address Range
55	32	1F8000h-1FFFFFh
54	32	1F0000h-1F7FFFh
53	32	1E8000h-1EFFFFh
52	32	1E0000h-1E7FFFh
51	32	1D8000h-1DFFFFh
50	32	1D0000h-1D7FFFh
49	32	1C8000h-1CFFFFh
48	32	1C0000h-1C7FFFh
47	32	1B8000h-1BFFFFh
46	32	1B0000h-1B7FFFh
45	32	1A8000h-1AFFFFh
44	32	1A0000h-1A7FFFh
43	32	198000h-19FFFFh
42	32	190000h-197FFFh
41	32	188000h-18FFFFh
40	32	180000h-187FFFh
39	32	178000h-17FFFFh
38	32	170000h-177FFFh
37	32	168000h-16FFFFh
36	32	160000h-167FFFh
35	32	158000h-15FFFFh
34	32	150000h-157FFFh
33	32	148000h-14FFFFh
32	32	140000h-147FFFh
31	32	138000h-13FFFFh
30	32	130000h-137FFFh
29	32	128000h-12FFFFh
28	32	120000h-127FFFh
27	32	118000h-11FFFFh
26	32	110000h-117FFFh
25	32	108000h-10FFFFh
24	32	100000h-107FFFh
23	32	0F8000h-0FFFFFh
22	32	0F0000h-0F7FFFh
21	32	0E8000h-0EFFFFh
20	32	0E0000h-0E7FFFh
19	32	0D8000h-0DFFFFh
18	32	0D0000h-0D7FFFh
17	32	0C8000h-0CFFFFh
16	32	0C0000h-0C7FFFh
15	32	0B8000h-0BFFFFh
14	32	0B0000h-0B7FFFh
13	32	0A8000h-0AFFFFh
12	32	0A0000h-0A7FFFh
11	32	098000h-09FFFFh
10	32	090000h-097FFFh
9	32	088000h-08FFFFh
8	32	080000h-087FFFh
7	32	078000h-07FFFFh
6	32	070000h-077FFFh
5	32	068000h-06FFFFh
4	32	060000h-067FFFh
3	32	058000h-05FFFFh
2	32	050000h-057FFFh
1	32	048000h-04FFFFh
0	32	040000h-047FFFh

Table 31. Bank A, Bottom Boot Block Addresses M36DR432BD

#	Size (KWord)	Address Range
14	32	038000h-03FFFFh
13	32	030000h-037FFFh
12	32	028000h-02FFFFh
11	32	020000h-027FFFh
10	32	018000h-01FFFFh
9	32	010000h-017FFFh
8	32	008000h-00FFFFh
7	4	007000h-007FFFh
6	4	006000h-006FFFh
5	4	005000h-005FFFh
4	4	004000h-004FFFh
3	4	003000h-003FFFh
2	4	002000h-002FFFh
1	4	001000h-001FFFh
0	4	000000h-000FFFh

APPENDIX B. COMMON FLASH INTERFACE

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 32, 33, 34 and 35 show the address used to retrieve each data. The Query data is always presented on the lowest order data outputs (DQ0-DQ7), the other outputs (DQ8-DQ15) are set to 0.

The CFI data structure contains also a security area starting at address 81h. This area can be accessed only in read mode and it is impossible to change after it has been written by ST. Issue a Read command to return to Read mode.

Table 32. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Table 33. CFI Query Identification String

Offset	Data	Description
00h	0020h	Manufacturer Code
01h	00A1h - bottom 00A0h - top	Device Code
02h-0Fh	reserved	Reserved
10h	0051h	Query Unique ASCII String "QRY"
11h	0052h	Query Unique ASCII String "QRY"
12h	0059h	Query Unique ASCII String "QRY"
13h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm
14h	0000h	
15h	offset = P = 0040h	Address for Primary Algorithm extended Query table
16h	0000h	
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)
18h	0000h	
19h	value = A = 0000h	Address for Alternate Algorithm extended Query table note: 0000h means none exists
1Ah	0000h	

Table 34. CFI Query System Interface Information

Offset	Data	Description
1Bh	0017h	V_{DDF} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Ch	0022h	V_{DDF} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Dh	0000h	V_{PPF} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PPF} pin is present
1Eh	00C0h	V_{PPF} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PPF} pin is present
1Fh	0004h	Typical timeout per single byte/word program (multi-byte program count = 1), 2^n µs (if supported; 0000h = not supported)
20h	0003h	Typical timeout for maximum-size multi-byte program or page write, 2^n µs (if supported; 0000h = not supported)
21h	000Ah	Typical timeout per individual block erase, 2^n ms (if supported; 0000h = not supported)
22h	0000h	Typical timeout for full chip erase, 2^n ms (if supported; 0000h = not supported)
23h	0003h	Maximum timeout for byte/word program, 2^n times typical (offset 1Fh) (0000h = not supported)
24h	0004h	Maximum timeout for multi-byte program or page write, 2^n times typical (offset 20h) (0000h = not supported)
25h	0002h	Maximum timeout per individual block erase, 2^n times typical (offset 21h) (0000h = not supported)
26h	0000h	Maximum timeout for chip erase, 2^n times typical (offset 22h) (0000h = not supported)

Table 35. Device Geometry Definition

Offset Word Mode	Data	Description
27h	0016h	Device Size = 2^n in number of bytes
28h	0001h	Flash Device Interface Code description: Asynchronous x16
29h	0000h	
2Ah	0000h	Maximum number of bytes in multi-byte program or page = 2^n
2Bh	0000h	
2Ch	0002h	Number of Erase Block Regions within device bit 7 to 0 = x = number of Erase Block Regions Note: 1. x = 0 means no erase blocking, i.e. the device erases at once in "bulk." 2. x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128KB device (1Mb) having blocking of 16KB, 8KB, four 2KB, two 16KB, and one 64KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions. 3. By definition, symmetrically block devices have only one blocking region.
M36DR432AD	M36DR432AD	Erase Block Region Information
2Dh	003Eh	bit 31 to 16 = z, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128 byte block size. e.g. for 64KB block size, z = 0100h = 256 => 256 * 256 = 64K
2Eh	0000h	
2Fh	0000h	
30h	0001h	bit 15 to 0 = y, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region: e.g. y = D15-D0 = FFFFh => y+1 = 64K blocks [maximum number] y = 0 means no blocking (# blocks = y+1 = "1 block") Note: y = 0 value must be used with number of block regions of one as indicated by (x) = 0
31h	0007h	
32h	0000h	
33h	0020h	
34h	0000h	
M36DR432AD	M36DR432AD	
2Dh	0007h	
2Eh	0000h	
2Fh	0020h	
30h	0000h	
31h	003Eh	
32h	0000h	
33h	0000h	
34h	0001h	

REVISION HISTORY

Table 36. Document Revision History

Date	Version	Revision Details
15-Jan-2003	1.0	First issue.
15-Jan-2003	1.1	Bottom Device Code corrected on page 1.
25-Feb-2003	2.0	Document promoted from Preliminary Data to full Datasheet status.
28-Feb-2003	2.1	V_{DDQF} signal removed from datasheet. SRAM Input Rise and Fall Times added to, and V_{DDF} and V_{DDS} parameters differentiated in Table 14, Operating and AC Measurement Conditions. V_{DDS} added to the SIGNAL DESCRIPTIONS section.