MITSUBISHI ELECTRIC

<Dual-In-Line Package Intelligent Power Module>

MINI DIPIPM Ver.4 Series APPLICATION NOTE PS21765 / PS21767 / PS21767-V

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CHAPTER 1 Mini DIPIPM Ver.4 INTRODUCTION

1.1 Target Applications

Motor drives for household equipment such as air conditioners, hot water system and low power industrial equipments.

1.2 Product Line-up

Table 1-1. Mini DIPIPM Ver.4 Line-up

Type Name	IGBT Rating	Motor Rating [1)]	Isolation Voltage
PS21765	20A/600V	1.5kW/220V_{AC}	V_{iso} = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS21767/-V [2)]	30A/600V	2.2kW/220V_{AC}	

Note 1: The motor ratings are simulation results under following conditions: V_{AC}=220V, V_D=V_{DB}=15V, Tc=100°C, Tj=125°C, f_{PWM}=5kHz, P.F=0.8, motor efficiency=0.75, current ripple ratio=1.05, motor over load 150% 1min.
Note 2: PS21767-V is faster switching type.

1.3 Functions and Features

Mini DIPIPM Ver.4 is an ultra-small compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC100-200V class low power motor inverter control. Fig.1-1, Fig.1-2 and Fig.1-3 show the photograph, internal cross-section structure and the circuit block diagram respectively.

One of the most important features of Mini DIPIPM Ver.4 is that realized higher thermal dissipation by built-in thermal structure with high thermal conductive insulated sheet, due to which, the chip shrinking becomes possible and therefore achieved super small package with lower temperature rise than previous DIPIPM.

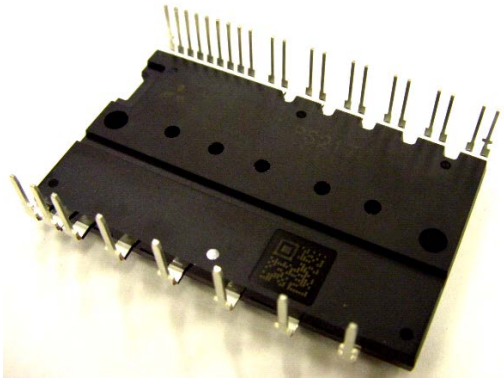


Fig.1-1 Package photograph

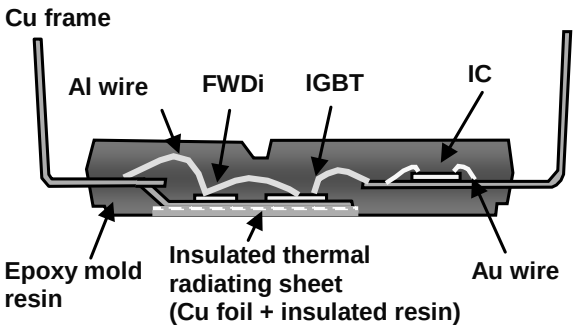


Fig.1-2 Internal cross-section structure

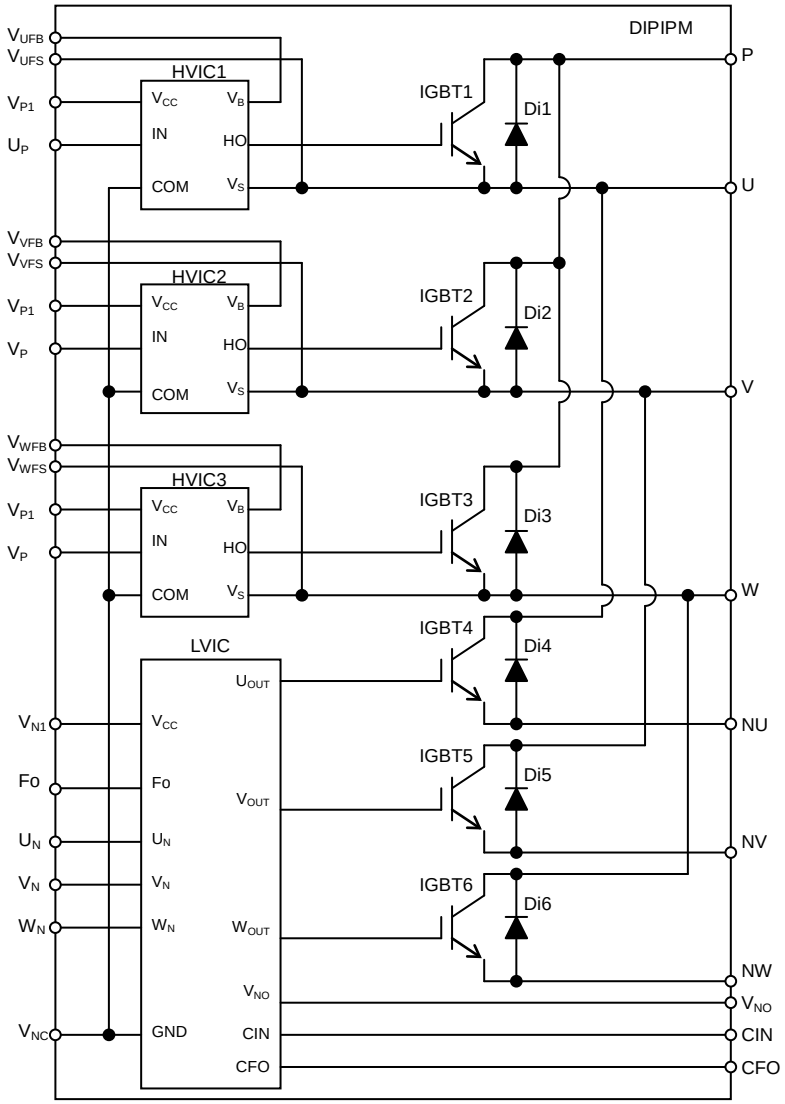


Fig.1-3 Internal circuit schematic

Features:

- For P-side IGBTs:
  -Drive circuit;
  -High voltage level shift circuit;
  -Control supply under voltage (UV) lockout circuit (without fault signal output).
- For N-side IGBTs:
  -Drive circuit;
  -Short circuit (SC) protection circuit (by using external shunt resistor)
  -Control supply under voltage (UV) lockout circuit (with fault signal output)
- Fault Signal Output
  -Corresponding to N-side IGBT SC protection, N-side UV protection and OT.
- IGBT Drive Supply
  -Single DC15V power supply.
- Control Input Interface
  -Schmitt-triggered 3V,5V input compatible, high active logic.
- UL recognized
  -UL1557 File E80276

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Mini DIPIPM Ver.4 Specifications

The Mini DIPIPM Ver.4 specifications are described below by using PS21767(30A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS21767 are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS21767

Inverter Part:

Item	Symbol	Condition	Rating	Unit	
Supply voltage	V_{CC}	Applied between P-NU,NV,NW	450	V	(1)
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-NU,NV,NW	500	V	(2)
Collector-emitter voltage	V_{CES}		600	V	(3)
Each IGBT collector current	$\pm I_C$	Tc=25°C	30	A	(4)
Each IGBT collector current (peak)	$\pm I_{CP}$	Tc=25°C, less than 1ms	60	A	
Collector dissipation	P_C	Tc=25°C, per 1 chip	90.9	W	
Junction temperature	Tj		-20~+150	°C	(5)

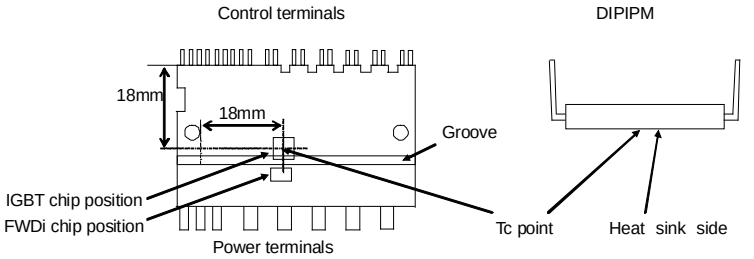
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS} ,V_{WFB}-V_{WFS}	20	V
Input voltage	V_{IN}	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}	-0.5~V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit	
Supply voltage self protection limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V	(6)
Module case operation temperature	Tc	(Note2)	-20~+100	°C	
Storage temperature	Tstg		-40~+125	°C	
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minutes, All connected pins to heat-sink plate	2500	Vrms	

(Note1) Tc measurement position



(7)

Item explanation:

(1) Vcc The maximum voltage can be biased between P-N in the steady state. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.

(2) Vcc(surge) The maximum P-N surge voltage is generated in switching state. A snubber circuit is necessary if P-N voltage exceeds Vcc(surge).

(3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.

(4) +/-I_C The allowable DC current continuously can flow at Tc=25°C.

(5) Tj The maximum junction temperature rating is 150°C.But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetive temperature variation ΔTj affects the life time of power cycle.

(6) Vcc(prot) The maximum supply voltage for IGBT when it can turn off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.

(7) Tc position Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS21767.

Table 2-2 Thermal resistance of PS21767

Thermal Resistance :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance (Note 2)	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	1.1	K/W
	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	-	-	2.8	

(Note 2) Grease with good thermal conductivity and long-term quality should be applied evenly with +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3K/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/mk

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10s is called as transient thermal impedance which is shown in Fig.2-1. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)

For example, the IGBT transient thermal impedance of PS21767 in 0.2s is 1.1×0.8=0.88K/W.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (e.g. In the cases at motor starting, at motor lock・・・)

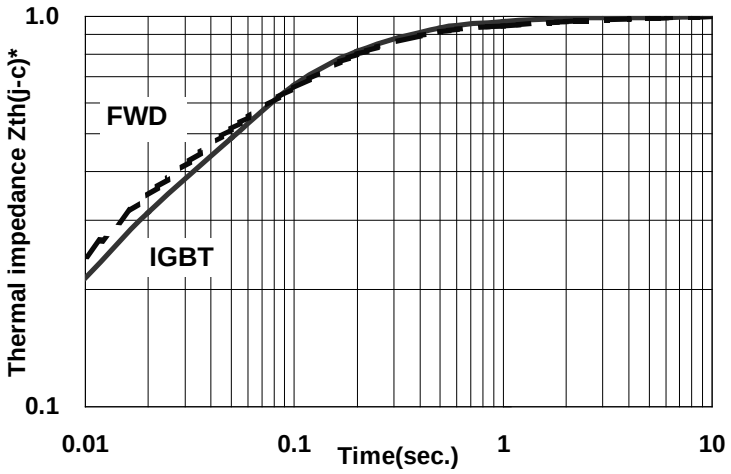


Fig.2-1 Typical transient thermal impedance

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS21767.

Table 2-3 Static characteristics and switching characteristics of PS21767

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_D=V_{DB}=15V	Tj=25°C	-	1.60	2.10	V
		I_C=30A, V_{IN}=5V	Tj=125°C	-	1.70	2.20	
FWDi forward voltage	V_{EC}	-I_C=30A, V_{IN}=0V		-	1.50	2.00	V
Switching times	t_{on}	V_{CC}=300V, V_D=V_{DB}=15V		0.70	1.30	1.90	μs
	t_{rr}	I_C=30A		-	0.30	-	
	$t_{c(on)}$	Tj=125°C		-	0.50	0.80	
	t_{off}	Inductive load		-	1.50	2.10	
	$t_{c(off)}$	V_{IN}=0-5V		-	0.40	0.60	
Collector-emitter cut-off current	I_{CES}	V_{CE}=V_{CES}	Tj=25°C	-	-	1	mA
			Tj=125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

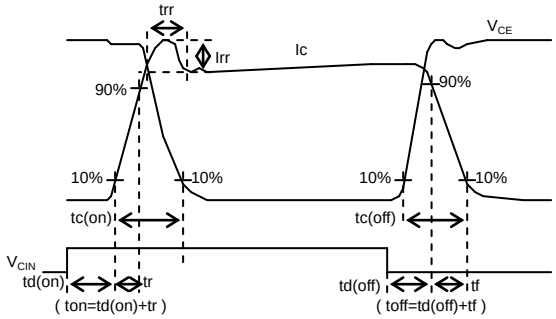


Fig.2-2 Switching time definition

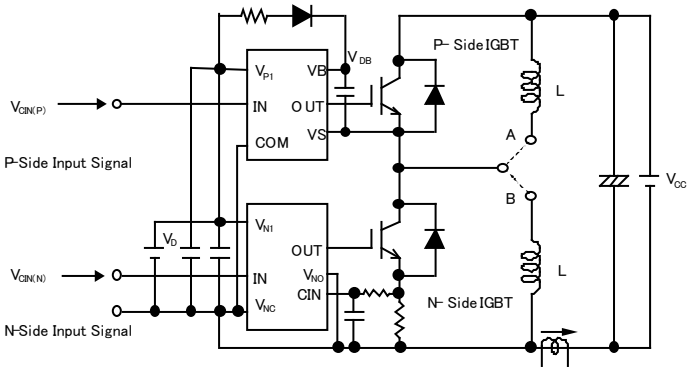
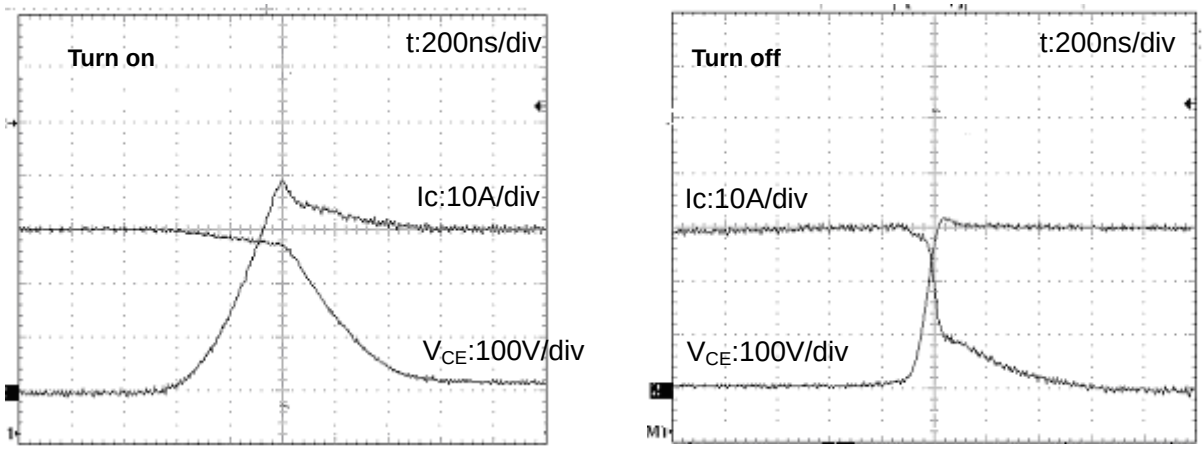


Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation



Conditions : V_{CC}=300V, V_D=V_{DB}=15V, Tj=125°C, Ic=30A, Inductive load half-bridge circuit

Fig.2-4 Typical switching waveform (PS21767)

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS21767

Control (Protection) Part:

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	V_D=V_{DB}=15V, V_{IN}=5V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	7.00	mA
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	-	-	0.55	
		V_D=V_{DB}=15V, V_{IN}=0V	Total of V_{P1}-V_{NC},V_{N1}-V_{NC}	-	-	7.00	
			V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	0.55	
Fo output voltage	V_{FOH}	V_{SC}=0V,Fo terminal pull-up to 5V by 10kΩ		4.9	-	-	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		-	-	0.95	
Short circuit trip level	$V_{SC(ref)}$	V_D=15V (Note3)		0.43	0.48	0.53	V
Input current	I_{IN}	V_{IN}=5V		1.0	1.5	2.0	mA
Supply circuit under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	10.0	-	12.0	V
	UV_{DBr}		Reset level	10.5	-	12.5	
	UV_{Dt}		Trip level	10.3	-	12.5	
	UV_{Dr}		Reset level	10.8	-	13.0	
Fault output pulse width	t_{FO}	C_{FO}=22nF (Note4)		1.0	1.8	-	ms
ON threshold voltage	$V_{th(on)}$	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}		-	2.3	2.6	V
OFF threshold voltage	$V_{th(off)}$			0.8	1.4	-	
ON/OFF threshold hysteresis voltage	$V_{th(hys)}$			0.5	0.9	-	

(Note 3) Short circuit protection is functioning only at the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

(Note 4) Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO} according to the following approximate equation :
C_{FO}= 12.2 × 10^{-6} × t_{FO} [F]

2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS21767 are given in Table 2-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

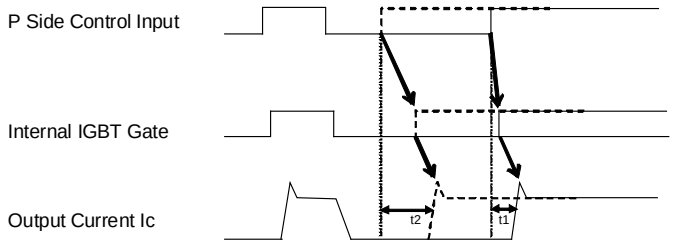
Table 2-5 Recommended operating conditions of PS21767

Recommended Operation Conditions

Item	Symbol	Condition		Recommended Min.	Recommended Typ.	Recommended Max.	Unit
Supply voltage	V_{CC}	Applied between P-NU,NV,NW		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
Control supply variation	ΔV_D, ΔV_{DB}			-1	-	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tc≤100°C		2.0	-	-	μs
PWM input frequency	f_{PWM}	Tc≤100°C, Tj≤125°C		-	-	20	kHz
Output r.m.s. current	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tc≤100°C (Note 7)	f_{PWM}=5kHz	-	-	21	Arms
			f_{PWM}=15kHz	-	-	16	
Minimum input pulse width	PWIN(on)	(Note 8)		0.3	-	-	μs
	PWIN(off)	200V≤V_{CC}≤350V, 13.5V≤V_D≤16.5V, 13.0V≤V_{DB}≤18.5V, -20°C≤Tc≤100°C, N-line wiring inductance less than 10nH (Note 9)	Below rated current	1.5	-	-	
			Between rated current and 1.7 times of rated current	3.0	-	-	
			Between 1.7 times and 2.0 times of rated current	3.6	-	-	
V_{NC} voltage variation	V_{NC}	Between V_{NC}-NU,NV,NW (including surge)		-5.0	-	5.0	V
Junction temperature	Tj			-20	-	125	°C

(Note 7) The allowable r.m.s. current value depends on the actual application conditons.
(Note 8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note 9) IPM might make delayed response (less than about 2μs) or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed responce.

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P side only)



Real line…off pulse width＞PWIN(off); turn on time t1
Broken line…off pulse width＜PWIN(off); turn on time t2

About control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

dV/dt ≤ +/-1V/μs, Vripple≤2Vp-p

2.1.6 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-6

Please refer to Section 2.4 for the detailed mounting instruction of Mini DIPIPM Ver.4.

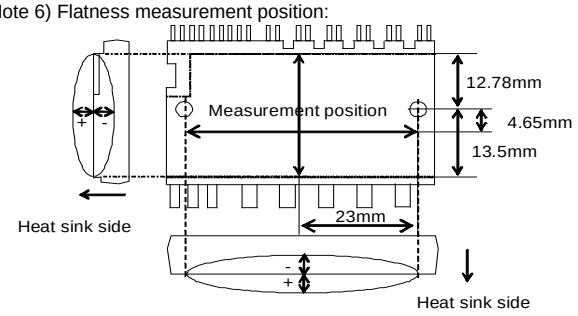
Table 2-6 Mechanical characteristics and ratings of PS21767

Mechanical Characteristics and Ratings

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3 (Note 5)	Recommended: 0.78N·m	0.59	–	0.98	N·m
Weight			–	21	–	g
Heat-sink flatness	(Note 6)		–50	–	100	μm

(Note 5) Plain washers (ISO 7089~7094) are recommended.

(Note 6) Flatness measurement position:



2.2 Protective Functions and Operating Sequence

Mini DIPIPM Ver.4 has the protection function that are SC protection and UV protection. Their operating principle and sequence are described below.

2.2.1 Short Circuit Protection

Mini DIPIPM Ver.4 uses external shunt resistor for the current detection as shown in Fig.2-5. The protection circuit inside the IC captures the excessive large current by comparing the CIN voltage feedback from the shunt with the referenced SC trip voltage, and perform protection automatically. The threshold voltage level of the SC protection is 0.48V(typ.).

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output.

To prevent DIPIPM erroneous protection due to the switching noise at normal operation and/or recovery current, it is necessary to set an RC filter(time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-5, 2-6). Also, please make the pattern wiring around the shunt resistor as short as possible.

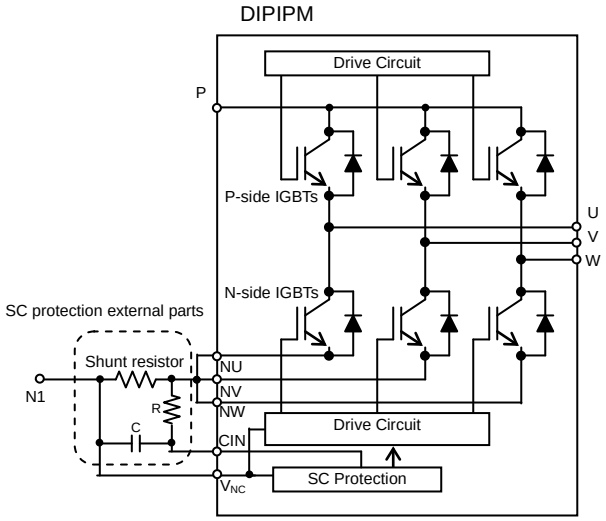


Fig.2-5 SC protecting circuit

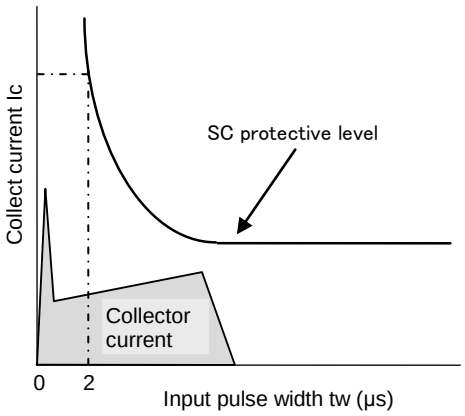


Fig.2-6 Filter time constant setting

SC protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and carrying current.
a2. Short circuit detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. Fo timer operation starts. The pulse width of the Fo signal is set by the external capacitor C_{FO}.
a6. Input = “L”. IGBT OFF.
a7. Input = “H”. But IGBT is still OFF state during outputting Fo.
a8. IGBT turns ON when L→H signal is input after Fo is reset.

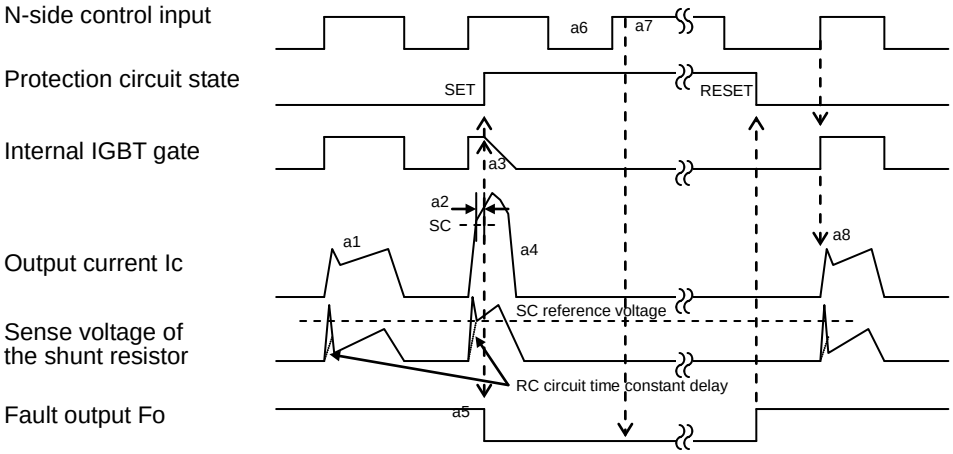


Fig.2-7 SC protection timing chart

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-7.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-7 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on.
4.0-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit will be destroyed.

Note: UV fault signals are asserted only for V_D supply.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, \quad Vripple \leq 2Vp\text{-}p$$

N-side UV Protection Sequence

b1. Control supply voltage V_D rises: After V_D level reaches under voltage reset level (UV_{Dr}), the circuits start to operate when next input is applied.
b2. Normal operation: IGBT turn on and carry current.
b3. V_D level falls to under voltage trip level. (UV_{Dt}).
b4. All N-side IGBTs turn OFF in spite of control input condition.
b5. Fo is output for the period determined by the capacitance C_{FO} but continuously during UV period.
b6. V_D level rises to UV_{Dr}.
b7. Normal operation: IGBT turn on and carry current.

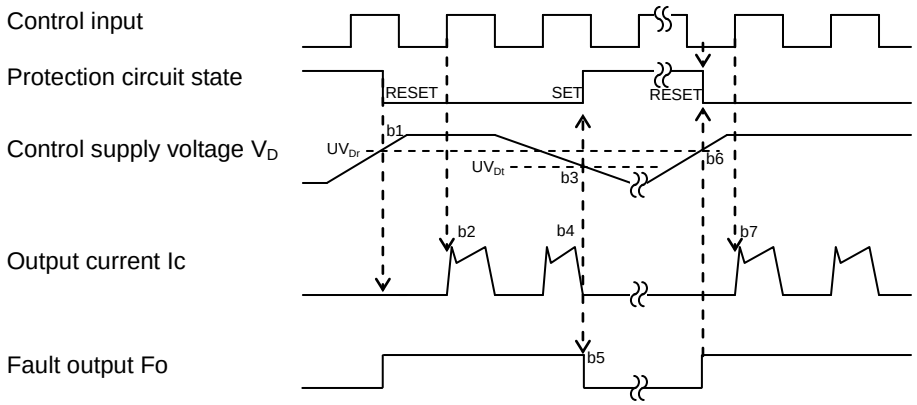


Fig.2-8 Timing chart of N-side UV protection

P-side UV Protection Sequence

c1. Control supply voltage rises: After the voltage level reaches UV_{DBr}, the circuits start to operate.
c2. Normal operation: IGBT turns on and carry current.
c3. V_{DB} level falls to under voltage trip level (UV_{DBt}).
c4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal output.
c5. V_{DB} level rises to UV_{DBr}.
c6. Normal operation: IGBT turns on and carries current.

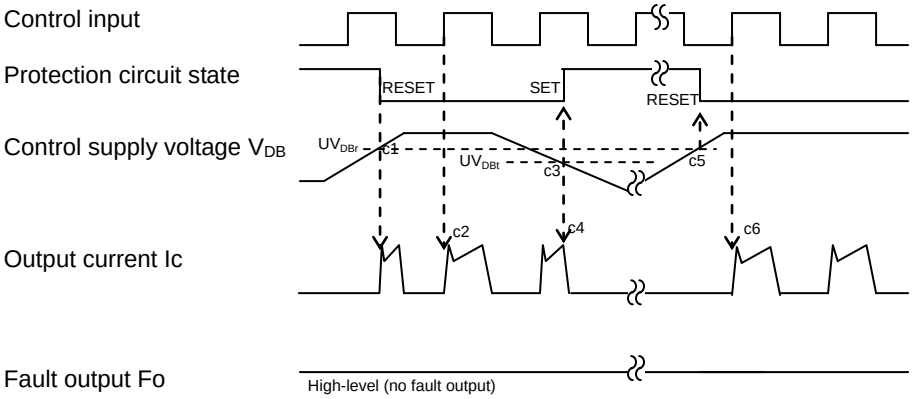


Fig.2-9 Timing Chart of P-side UV protection

2.3 Package Outlines

2.3.1 Package Outline Drawing

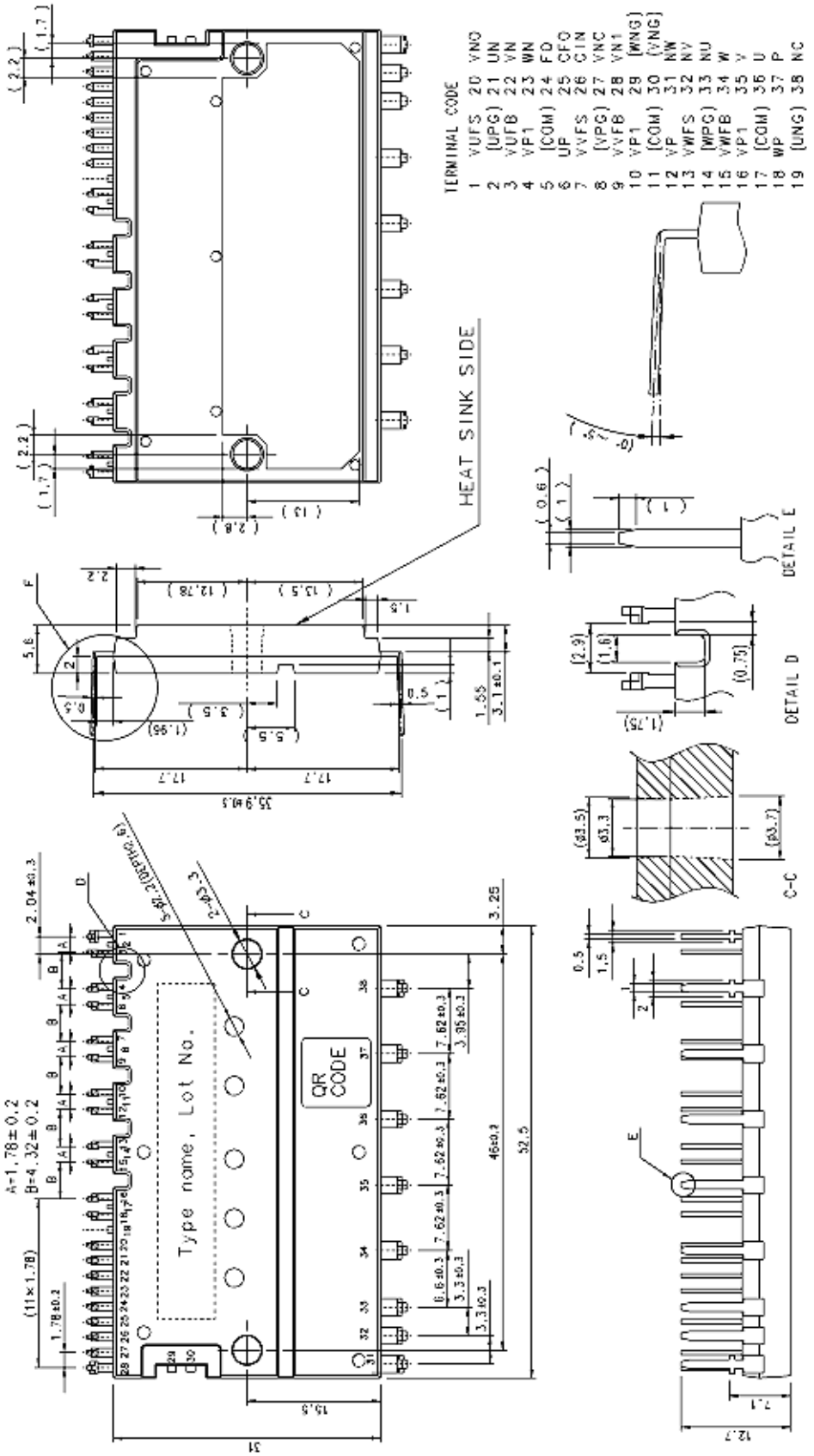
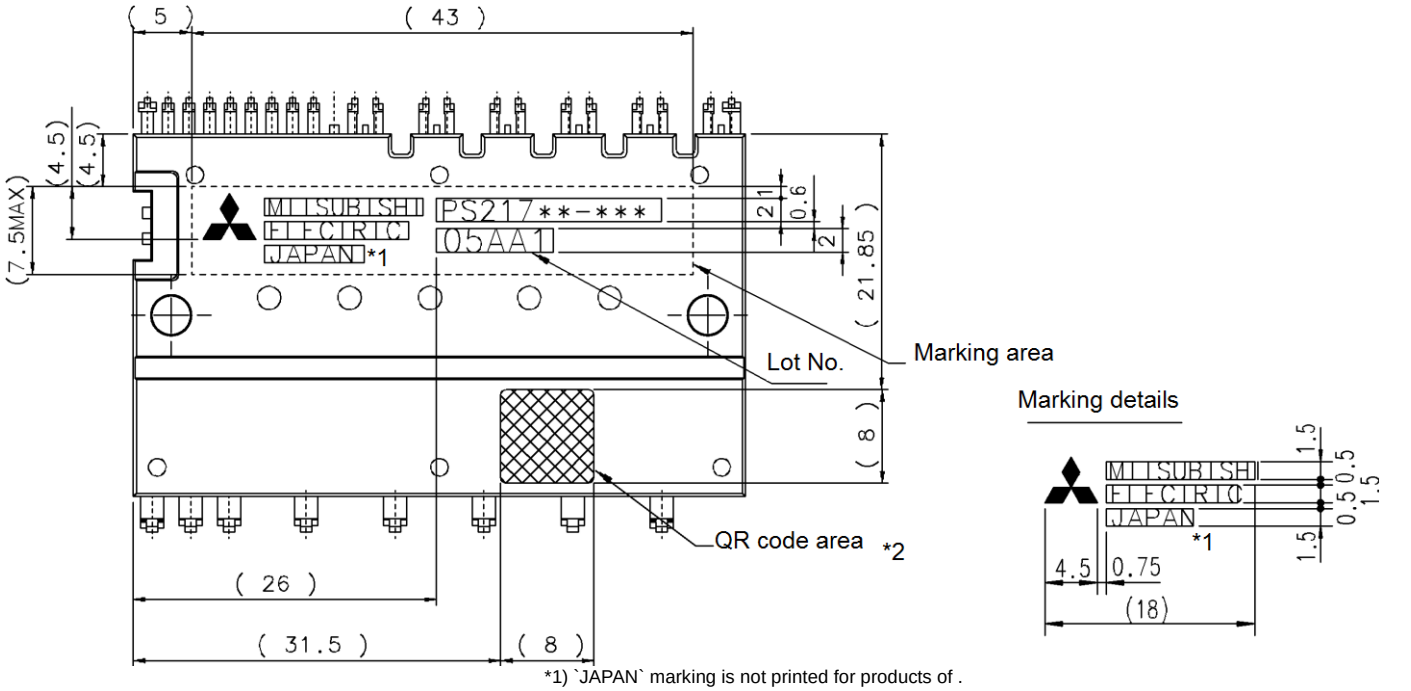


Fig.2-10 Package outline drawing

2.3.2 Laser Marking

The laser marking specification of Mini DIPIPM Ver.4 is described in Fig.2-11. Mitsubishi Corporation mark, Type name, Lot number, and QR code mark are marked in the upper side of module.



*1) `JAPAN` marking is not printed for products of .
*2) QR Code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.

Fig.2-11 Laser marking view

The Lot number indicates production year, month, and running number.
The detailed is described as below.

(1) Products of JAPAN

(Example) 1 2 A A1

- A1: Running number
- A: Product month (however O: October, N: November, D: December)
- 2: Last figure of Product year (e.g. '1' in the case of 201<u>1</u>)

(2) Products of CHINA

(Example) H 1 2 A A1

- A1: Running number
- A: Product month (however O: October, N: November, D: December)
- 2: Last figure of Product year (e.g. '1' in the case of 201<u>1</u>)
- 1: Factory Identification

2.3.3 Terminal Description

Table 2-8 Terminal description

Terminal No.	Terminal Name	Description
1	V_{UFS}	U-phase P-side drive supply GND terminal
2	UPG	Dummy-pin
3	V_{UFB}	U-phase P-side drive supply positive terminal
4	V_{P1}	U-phase P-side control supply positive terminal
5	COM	Dummy-pin
6	U_P	U-phase P-side control input terminal
7	V_{VFS}	V-phase P-side drive supply GND terminal
8	VPG	Dummy-pin
9	V_{VFB}	V-phase P-side drive supply positive terminal
10	V_{P1}	V-phase P-side control supply positive terminal
11	COM	Dummy-pin
12	V_P	V-phase P-side control input terminal
13	V_{WFS}	W-phase P-side drive supply GND terminal
14	WPG	Dummy-pin
15	V_{WFB}	W-phase P-side drive supply positive terminal
16	V_{P1}	W-phase P-side control supply positive terminal
17	COM	Dummy-pin
18	W_P	W-phase P-side control input terminal
19	UNG	Dummy-pin
20	VNO	N-side IGBT gate signal referenced GND terminal
21	U_N	U-phase N-side control input terminal
22	V_N	V-phase N-side control input terminal
23	W_N	W-phase N-side control input terminal
24	F_O	Fault signal output terminal
25	CFO	Fault pulse output width setting terminal
26	CIN	SC current trip voltage detecting terminal
27	V_{NC}	N-side control supply GND terminal
28	V_{N1}	N-side control supply positive terminal
29	WNG	Dummy-pin
30	VNG	Dummy-pin
31	NW	WN-phase IGBT emitter
32	NV	VN-phase IGBT emitter
33	NU	UN-phase IGBT emitter
34	W	W-phase output terminal
35	V	V-phase output terminal
36	U	U-phase output terminal
37	P	Inverter DC-link positive terminal
38	NC	No connection

Note) Dummy pin has some potential like gate voltage.
Don’t connect all dummy-pins to any other terminals or PCB pattern.

Table 2-9 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with good frequency characteristics should be mounted very closely to these terminals. • Design the supply carefully so that the voltage ripple caused by operation keep within the specification. ($dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$) • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
VNO terminal	V_{NO}	• The terminal for N-side IGBT gate signal reference.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. • Voltage input type. These terminals are internally connected to Schmitt trigger circuit and pulled down by min 2.5kΩ resistor internally • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Use RC coupling in case of signal oscillation. Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor.
Short-circuit trip voltage detecting terminal	CIN	• For short circuit protection, input the potential of external shuint resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal. • Fo signal line should be pulled up to the logic supply. (In the case pulling up to 5V supply, over 5kΩ resistor is needed for limitting the Fo sink current I_{Fo} up to 1mA. Normally 10kΩ is recommended.)
Fault pulse output width setting terminal	CFO	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and V_{NC}. • When 22nF is connected, then the Fo pulse width becomes 1.8ms. C_{FO} (F) = $12.2 \times 10^{-6} \times t_{FO}$ (Required Fo pulse width)
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side IGBT • Usually, these terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and assembling precautions of Mini DIPIPM Ver.4.

2.4.1 Electric Spacing

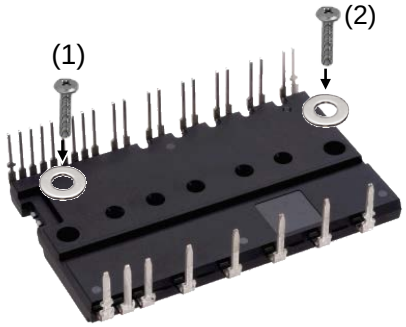
The electric spacing specification of Mini DIPIPM Ver.4 is shown in Table 2-10

Table 2-10 Minimum insulation distance of Mini DIPIPM Ver.4

Clearance(mm)		Creepage(mm)	
Between power terminals	4.0	Between power terminals	4.0
Between control terminals	2.5	Between control terminals	6.0
Between terminals and heat sink	3.0	Between terminals and heat sink	4.0

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the device. The recommended fastening procedure is shown in Fig.2-12. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-12 Recommended screw fastening order

Table 2-12 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 0.78N·m, Screw : M3	0.59	-	0.98	N·m
Flatness of outer heat sink	Refer Fig.2-13	-50	-	+100	μm

Note: Recommend to use plain washer (ISO7089-7094) in fastening the screws.

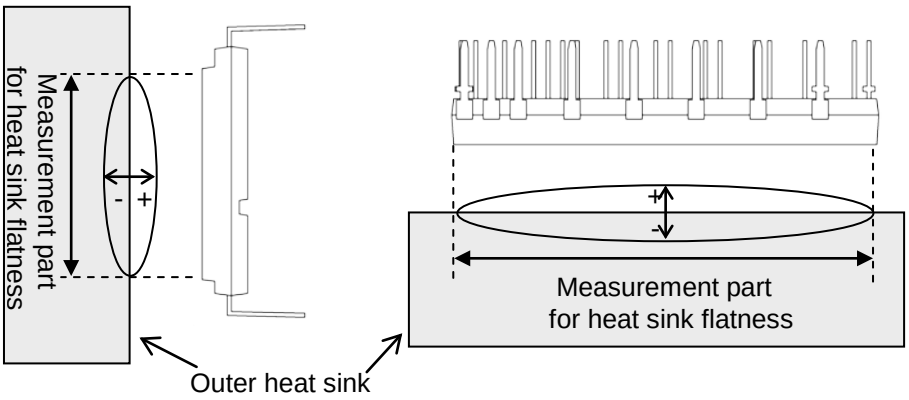


Fig.2-13 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in Table 2-12 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s. For pre-heat temperature, it is recommended to be below 125°C because of the maximum storage temperature of DIPIPM is 125°C.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-12 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since hand soldering condition depends on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous condition of hand soldering cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept below 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: Mini DIPIPM Ver.4

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

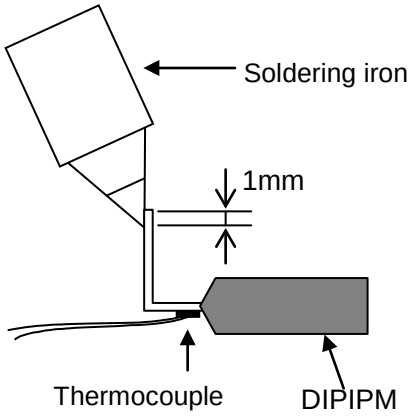


Fig.2-14 Heating and measuring point

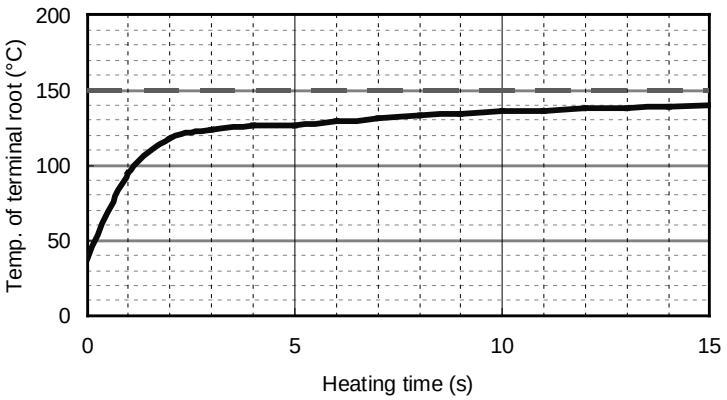


Fig.2-15 Temperature alteration of the terminal root (Typcal)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER 3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states the Mini DIPIPM Ver.4 application method and interface circuit design hints.

3.1.1 System connection

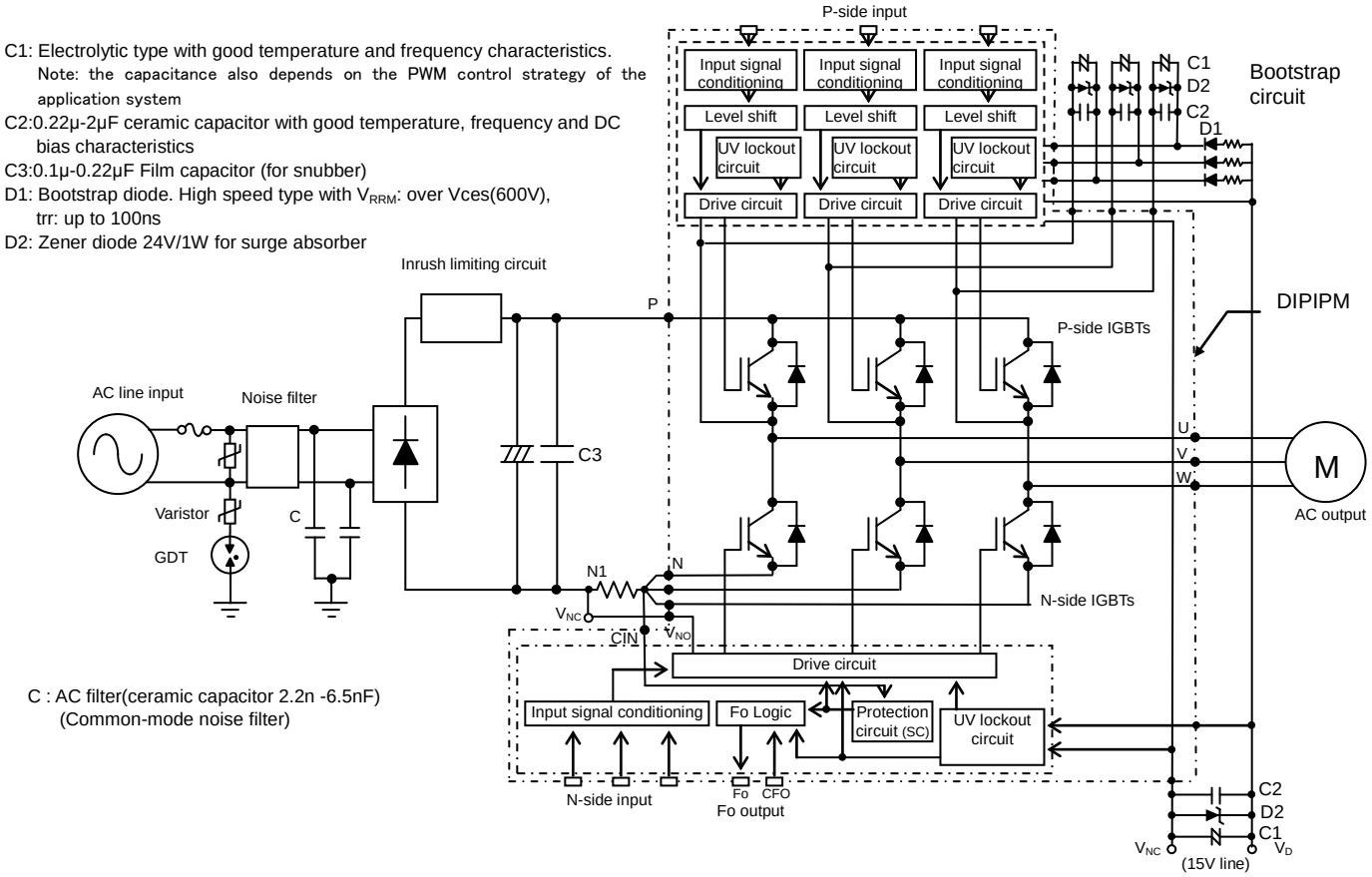


Fig.3-1 Application System block diagram of Mini DIPIPM Ver.4

3.1.2 Interface Circuit (Direct Coupling Interface. One shunt)

Fig.3-2 shows a typical application circuit of interface schematic, in which control signals are transfered directly from a controller (MCU or DSP).

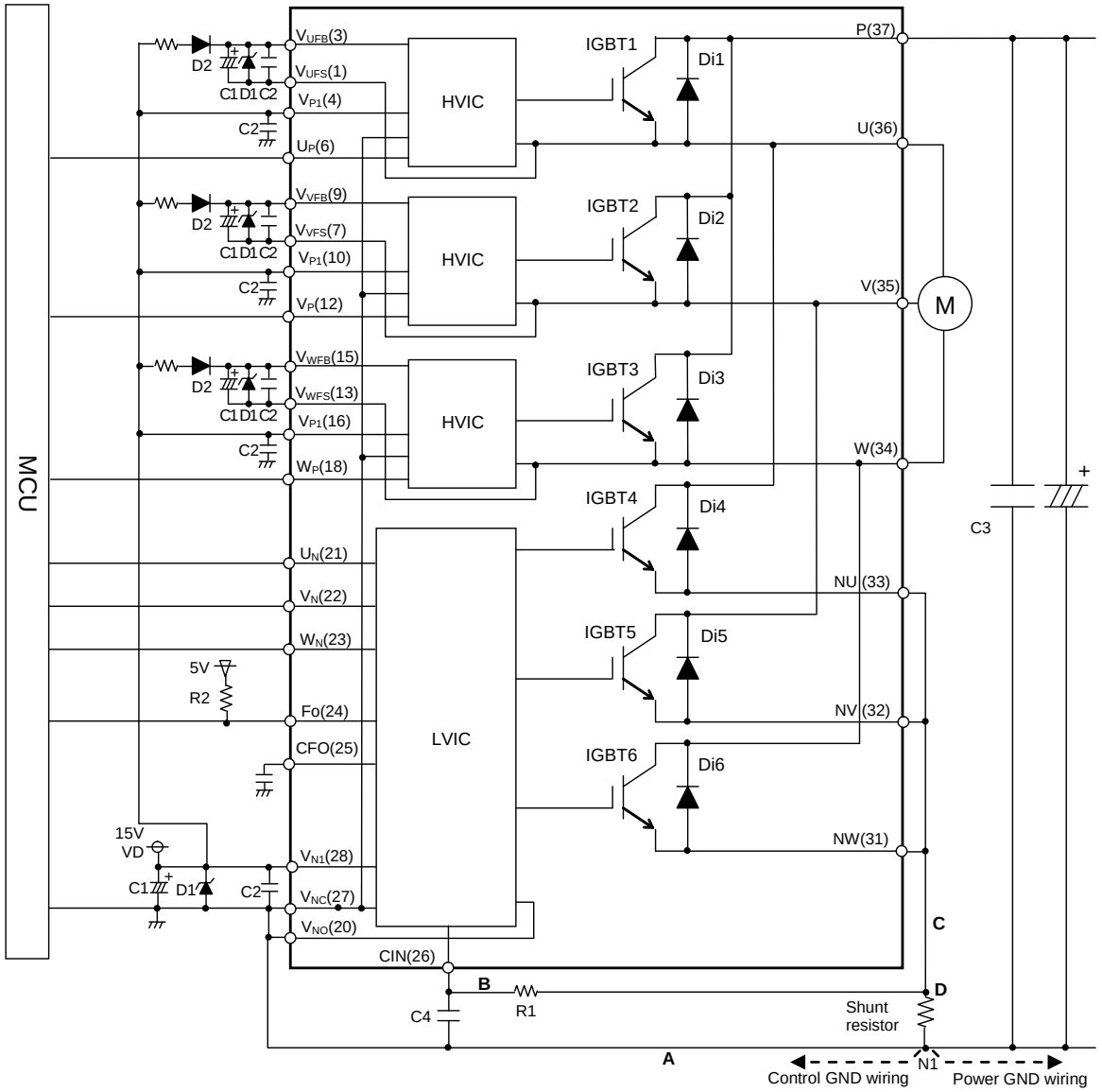


Fig.3-2 Interface circuit example (Direct coupling interface with one shunt resistor)

Note:

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).

(2) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1μ-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(3) The time constant R1C4 of the protection circuit is recommended to be in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4.

(4) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(5) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.

(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor.

(7) For shunt resistor, the variation within 1% (including temperature characteristics), low inductance SMD type is recommended.

(8) To prevent malfunction or surge destruction, the wiring of A, B, C should be as short as possible.

(9) Fo output is open drain type. It should be pulled up to control power supply (e.g. 5V) by a resistor that makes I_{Fo} up to 1mA. (In the case pulling up to 5V supply, over 5kΩ resistor is needed. Normally 10kΩ is recommended.)

(10) Fo pulse width can be set by the capacitor connected to CFO terminal. CFO(F) = 12.2 x 10^{-6} x t_{FO} (Required Fo pulse width).

(11) High voltage (V_{RRM} =600V or more) and fast recovery type (trr=100ns or less) diode D2 should be used for bootstrap circuit.

(12) Input drive is High-active type. There is a min. 2.5kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.Due to integrate the HVIC, direct coupling to MCU without isolation circuit is possible.

(13) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.

3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

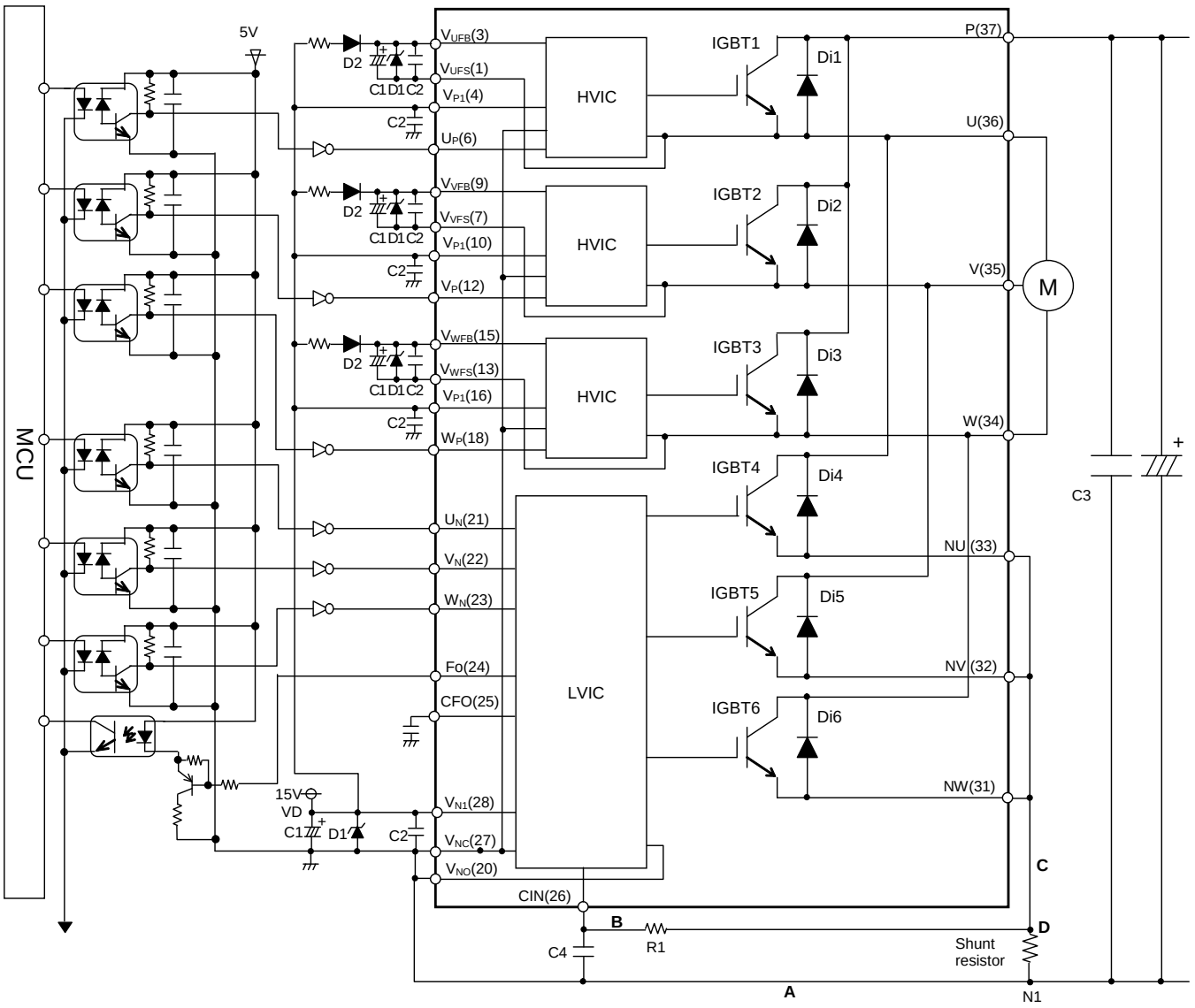


Fig.3-3 Interface circuit example with opto-coupler

Note:

(1) High speed (high CMR) opto-coupler is recommended.

(2) Max. Fo terminal sink current is 1mA. A buffer circuit is necessary to drive an opto-coupler.

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

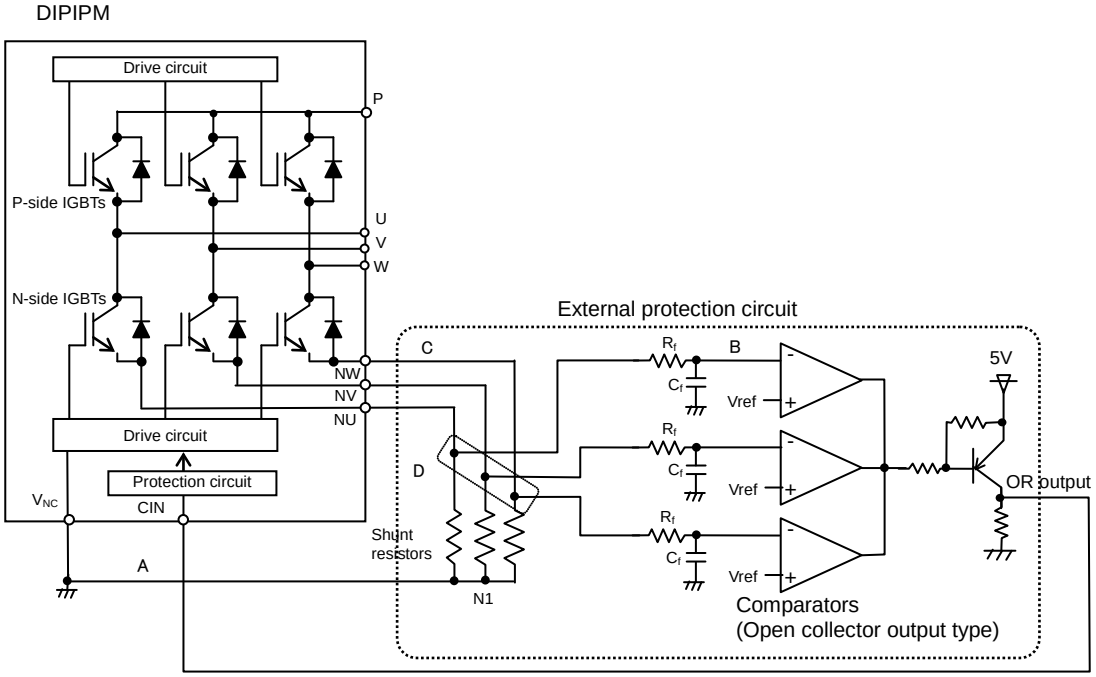


Fig.3-4 Interface Circuit example

Note:

(1) It is necessary to set the time constant R_fC_f of external comparator input so that IGBT can stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the shunt resistance so that SC trip-level is less than specified value.(2times of rating current for Mini DIPIPM Ver.4)
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.53V (=maximum Vsc(ref)).

3.1.5 Circuits of Signal Input terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIPIPM is high-active input logic.

Each input circuits of the DIPIPM has a 2.5kΩ(min) pull-down resistor as shown in Fig.3-5, so external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1, a direct coupling to 3V class microcomputer or DSP becomes possible.

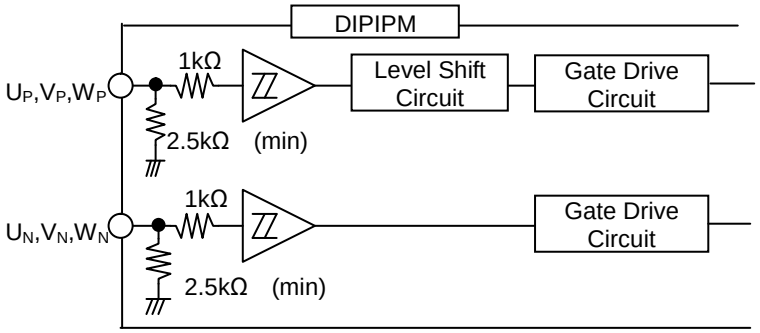


Fig.3-5. Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings(V_D=15V,Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals U_N,V_N,W_N-V_{NC} terminals	-	2.3	2.6	V
Turn-off threshold voltage	Vth(off)		0.8	1.4	-	
Threshold voltage hysterisis	Vth(hys)		0.5	0.9	-	

The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter.

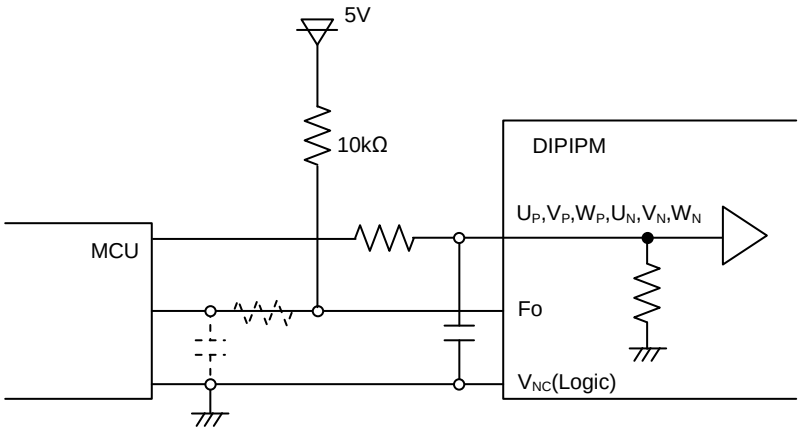


Fig.3-6 Control input connection

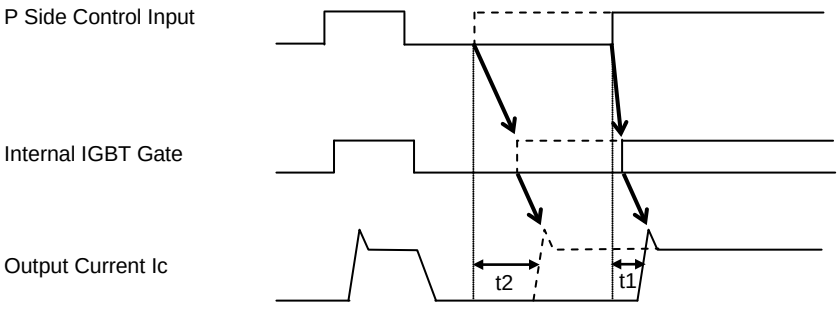
Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIPIPM signal input section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

There are limits for the minimum input pulse width in the DIPIPM. The DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Table 3-2)

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		PN	Min. value	Unit
On signal	PWIN(on)	-		PS21765	0.3	μs
				PS21767	0.3	
Off signal	PWIN(off)	$200 \leq V_{CC} \leq 350V$, $13.5 \leq V_D \leq 16.5V$, $13.5 \leq V_{DB} \leq 18.5V$, $-20 \leq T_C \leq 100°C$, N line wiring inductance less than 10nH	Up to rated current	PS21765	1.4	
				PS21767	1.5	
			From rated current to 1.7times of rated current	PS21765	2.5	
				PS21767	3.0	
			From 1.7 times to 2.0 times of rated current	PS21765	3.0	
				PS21767	3.6	

*) Input signal with ON pulse width less than PWIN(on) might make no response.
IPM might make delayed response (less than about 2μs) or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed responce.



Real line: off pulse width>PWIN(off); turn on time t1
Broken line: off pulse width<PWIN(off); turn on time t2
(t1:Normal switching time)

Fig.3-7 Delayed Response with shorter input off (P-side only)

(2) Internal Circuit of Fo Terminal

F_O terminal is open drain type, it should be pulled up to a 5V supply as shown in Fig.3-6. Fig.3-8 shows the typical V-I characteristics of Fo output. The maximum sink current of Fo output is 1mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler driving current.

Table 3-3 Electric characteristics of Fo output

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo=10kΩ,5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V,Fo=1mA	-	-	0.95	V

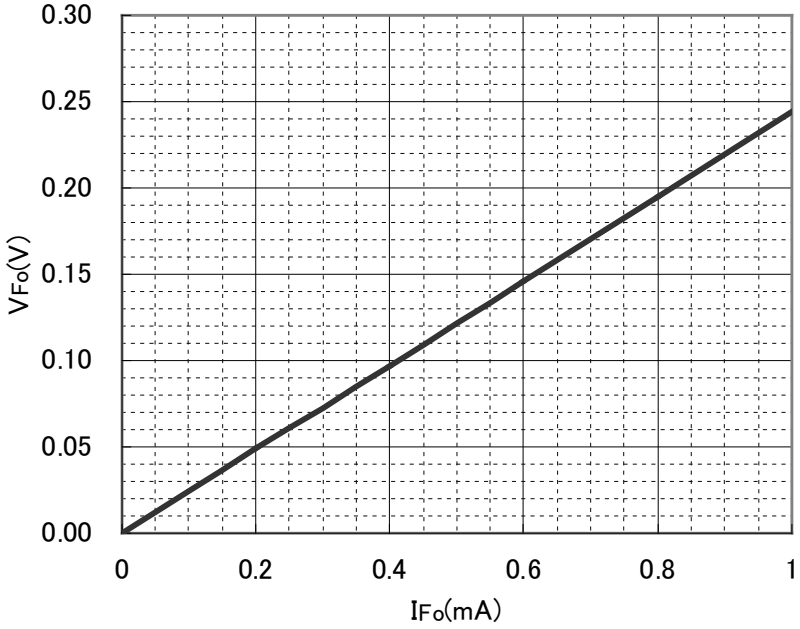


Fig.3-8 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.6 Snubber Circuit

In order to prevent DIPIPM from extra surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted between P and N terminals close to DIPIPM.

There are two positions (1) or (2) to mount a snubber capacitor as shown in Fig.3-9. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charge and discharge currents generated by the wiring inductance and the snubber capacitance will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) and part-B should be as small as possible. A better wiring example is shown in location (3).

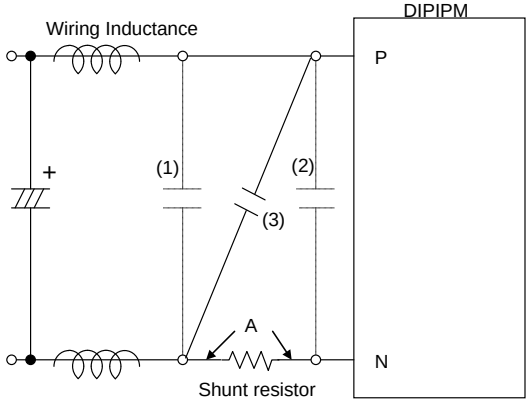
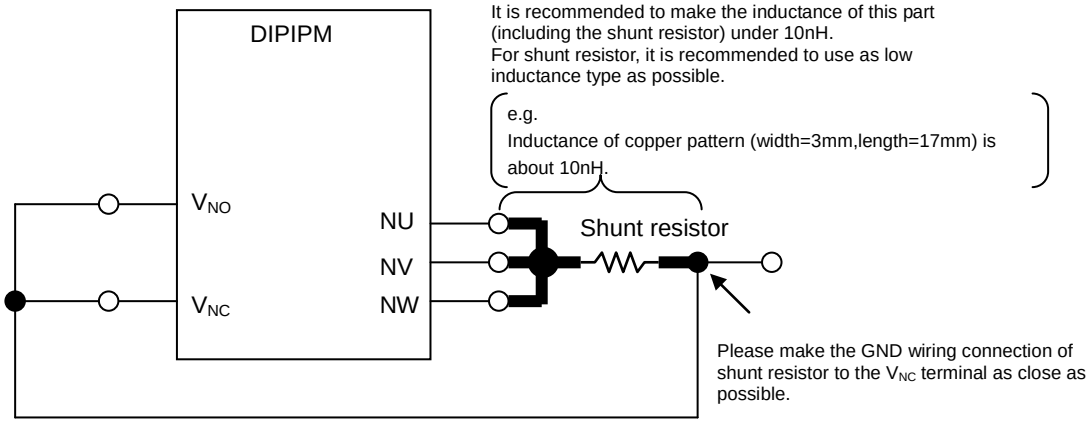


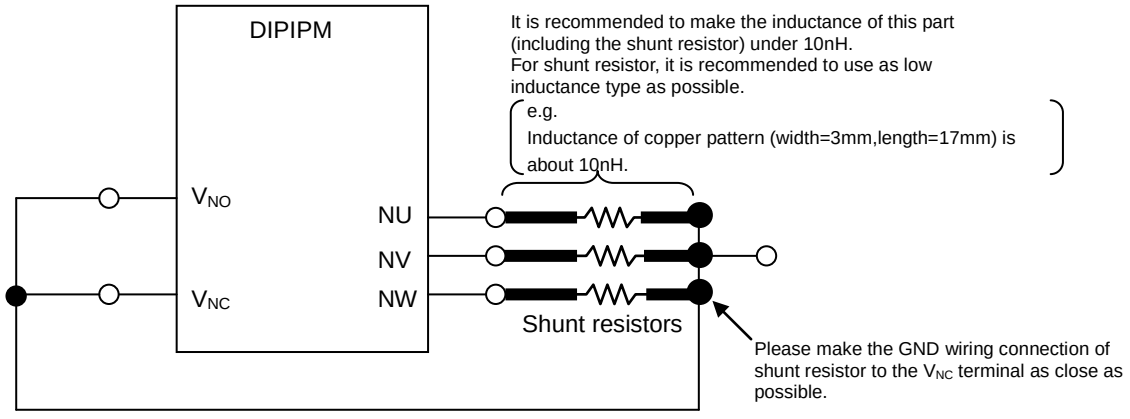
Fig.3-9 Recommended snubber circuit location

3.1.7 Recommended Wiring method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and DIPIPM might cause so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt and DIPIPM should be as short as possible and using low inductance type resistor such as SMD resistor instead of long-lead type resistor.



(a) Wiring instruction (For one shunt)



(b) Wiring instruction (For three shunts)

Fig.3-10 Recommended wiring method of shunt resistor

Influence of pattern wiring around the shunt resistor is shown below.

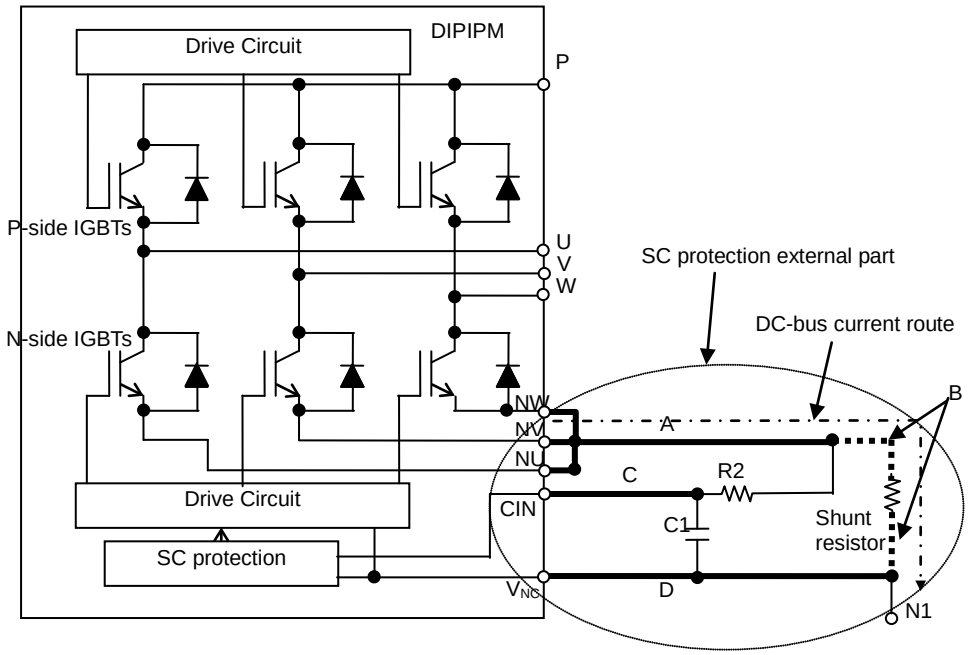


Fig.3-11 External protection circuit

(1) Influence of the part-A wiring

The ground of Low-side IGBT gate is V_{NC}. If part-A wiring pattern in Fig.3-11 is too long, extra voltage generated by the wiring parasitic inductor will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. Please install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.8 Precaution for wiring on PCB

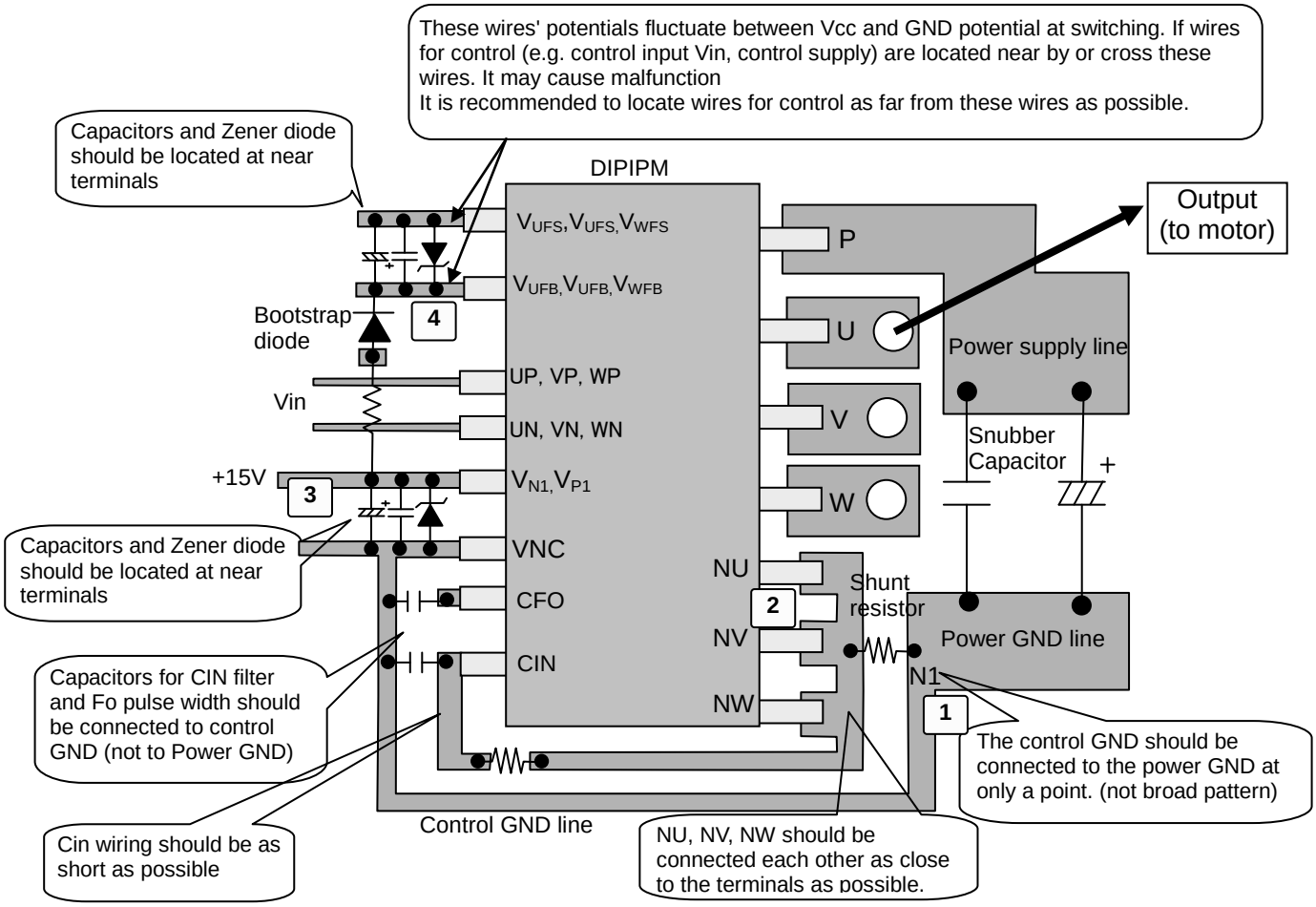


Fig.3-12 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Long pattern between NU, NV, NW terminals and N1(including inductance of shunt resistor)	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction by VS voltage (output terminal potential) decreasing excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	The cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then since the incorrect signals are input to DIPIPM input, the arm short might occur.

3.1.9 Parallel operation of DIPIPM

Fig.3-13 shows the circuitry of parallel connection of two DIPIPMs.

Route (1) and (2) indicate the gate charging path of low-side IGBT in DIPIPM No.1 & 2 respectively. In the case of DIPIPM 1, the parasitic inductance becomes large by long wiring and it might have a negative effect on DIPIPM's switching operation. (Charging of bootstrap capacitor for high-side might be affected similarly.) Also, such a wiring makes DIPIPM be affected by noise easily, then it might lead to malfunction. If more DIPIPMs are connected in parallel, GND pattern becomes longer and the influence to other circuit (power supply, protection circuit etc.) by the fluctuation of GND potential might occur. Therefore parallel connection is not recommended. Also because DIPIPM doesn't consider about the fluctuation of characteristics between each phases definitely, it cannot be recommended to drive same load by parallel connection with other phase IGBT or IGBT of other DIPIPM.

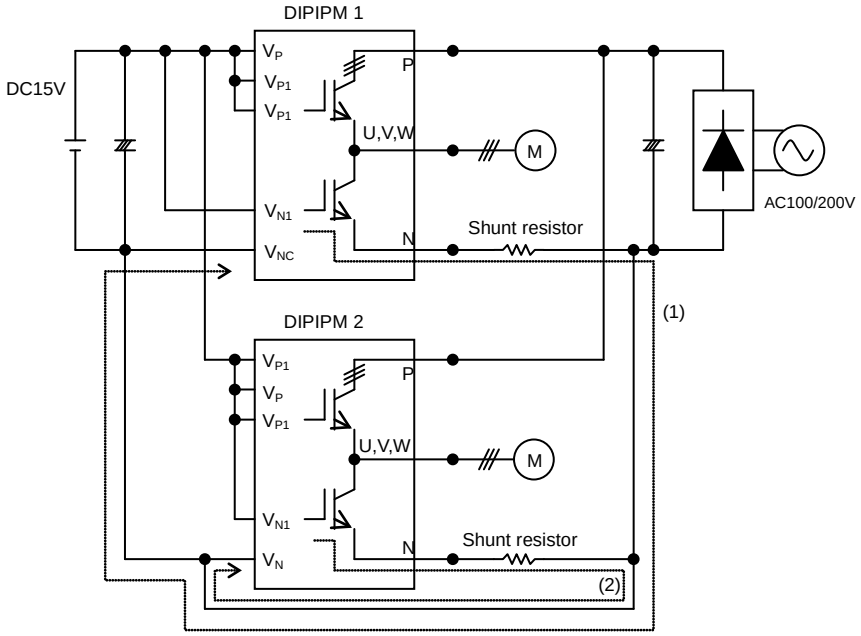


Fig.3-13 Parallel operation

3.1.10 SOA of Mini DIPIPM Ver.4

The following describes the SOA (Safety Operating Area) of the Mini DIPIPM Ver.4.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that DIPIPM can protect itself.

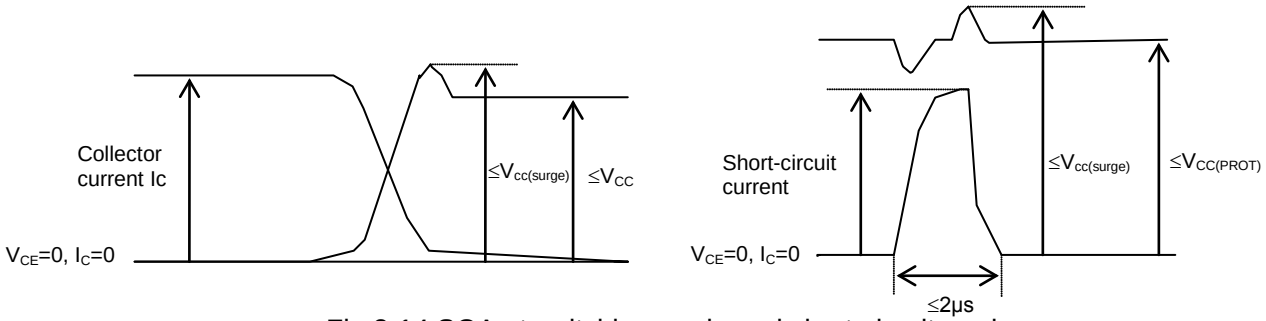


Fig.3-14 SOA at switching mode and short-circuit mode

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 400V.

3.1.11 SCSOA

Fig.3-15,16 shows the typical SCSOA performance curves example of PS21765,PS21767.

Conditions: Vcc=400V, Tj=125°C at initial state, Vcc(surge)≤500V(surge included), non-repetitive,2m load.

Fig.3-15 shows PS21765 can shutdown safely an SC current that is about 9 times of its current rating under the conditions only if the IGBT conducting period is less than 4.5μs.

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and so on, it is necessary to set time constant of RC filter with a margin.

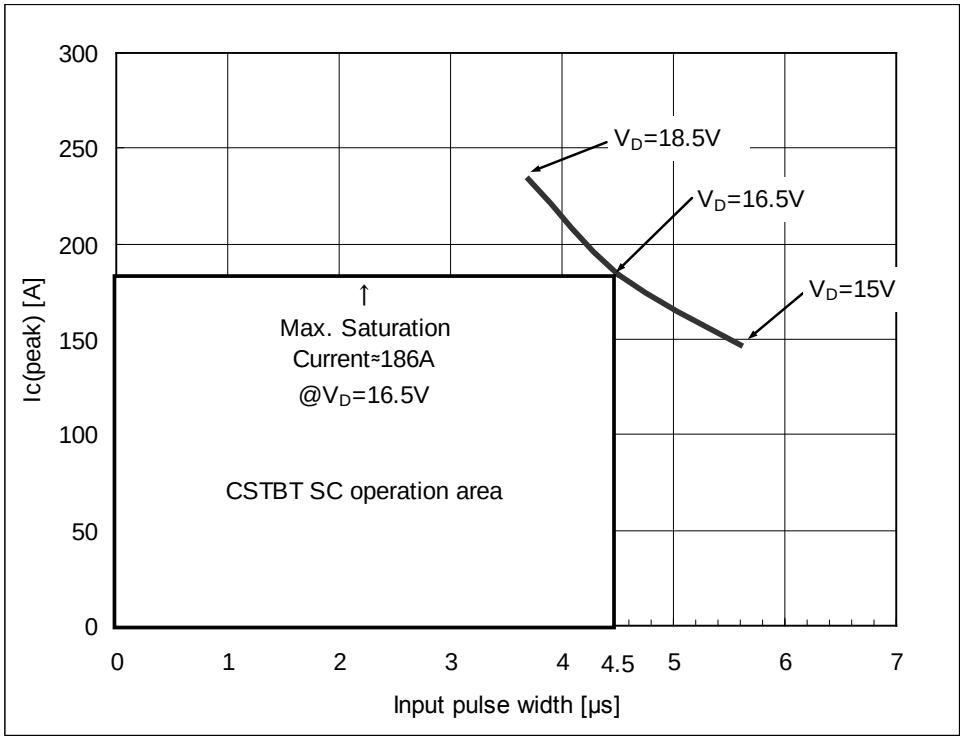


Fig.3-15 Typical SCSOA curve of PS21765

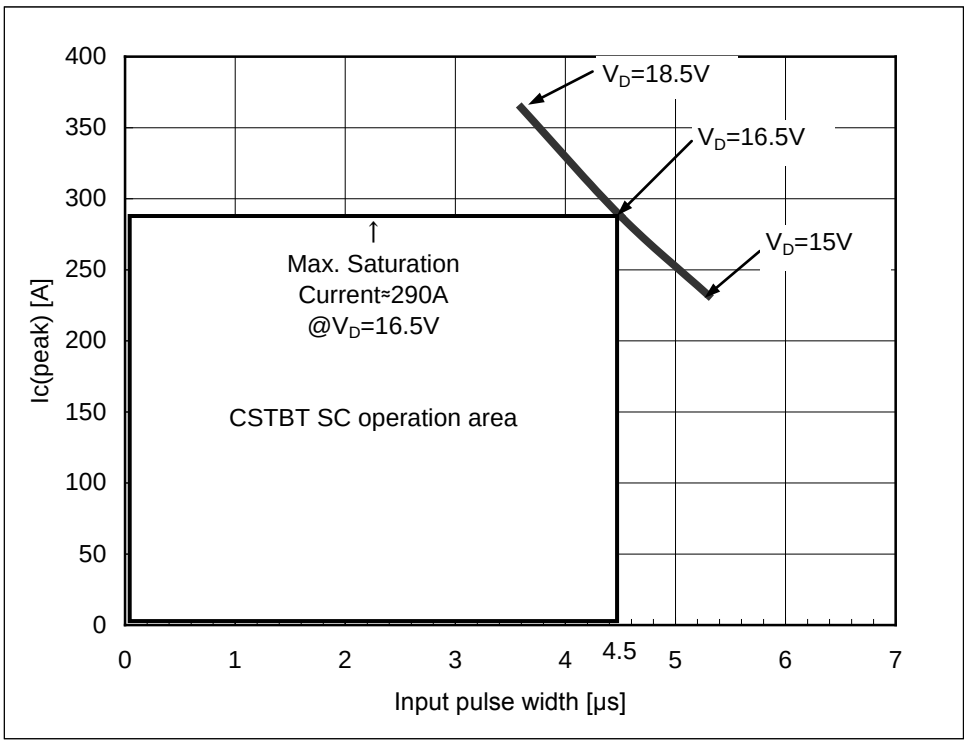


Fig.3-16 Typical SCSOA curve of PS21767

3.1.12 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.
Fig.3-17 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).
(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

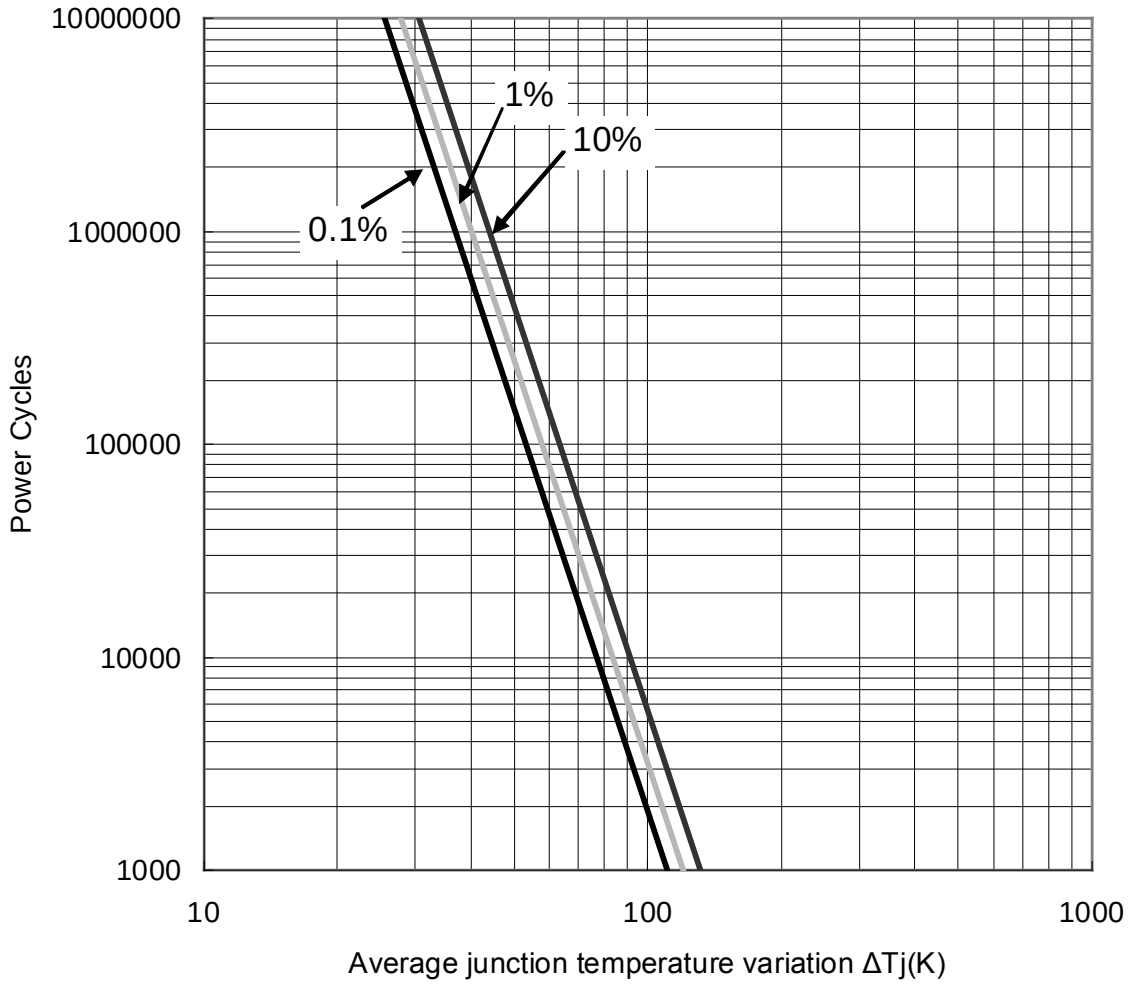


Fig.3-17 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\ Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\ Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\ Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\ Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\ Icp \times \sin x) + Psw(off)(@\ Icp \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-18, and its dynamic loss can be calculated by the following expression:

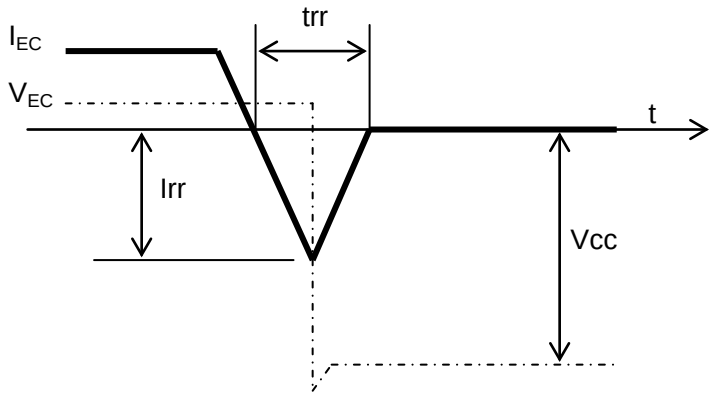


Fig.3-18 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\ Icp \times \sin x) \times Vcc \times trr(@\ Icp \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\ Icp \times \sin x) \times Vcc \times trr(@\ Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-19 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=300V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., Switching loss=Typ., Tj=125°C, Tf=100°C, Rth(j-f)=Max., Rth(c-f)=0.3°C/W (per 1/6 module), P.F=0.8, 3-phase PWM modulation, 60Hz sine waveform output

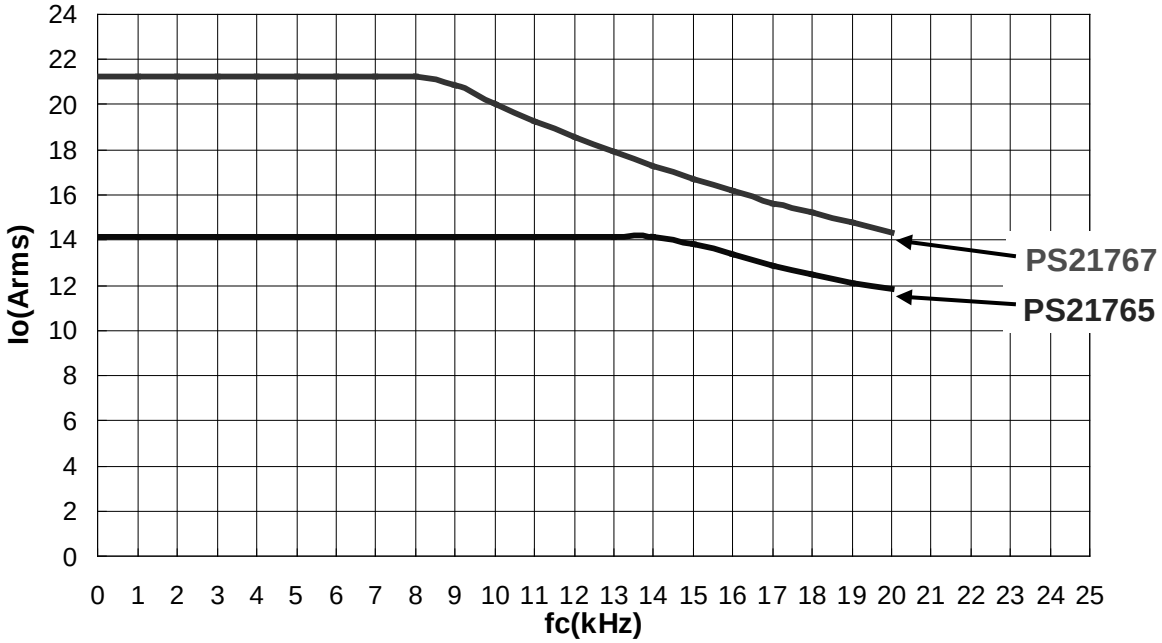


Fig.3-19 Effective current-carrier frequency characteristics

Fig.3-19 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tf=100°C. Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided at our web site. URL: http://www.MitsubishiElectric.com/semiconductors/

3.3 Noise Withstand Capability

3.3.1 Evaluation Circuit

Mini DIPIPM Ver.4 series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-20. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

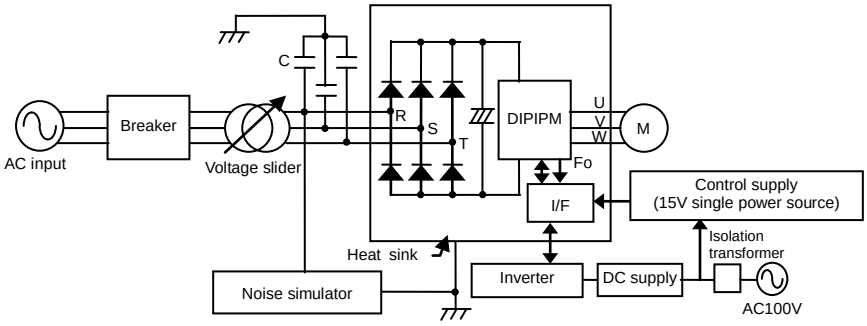


Fig.3-20 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

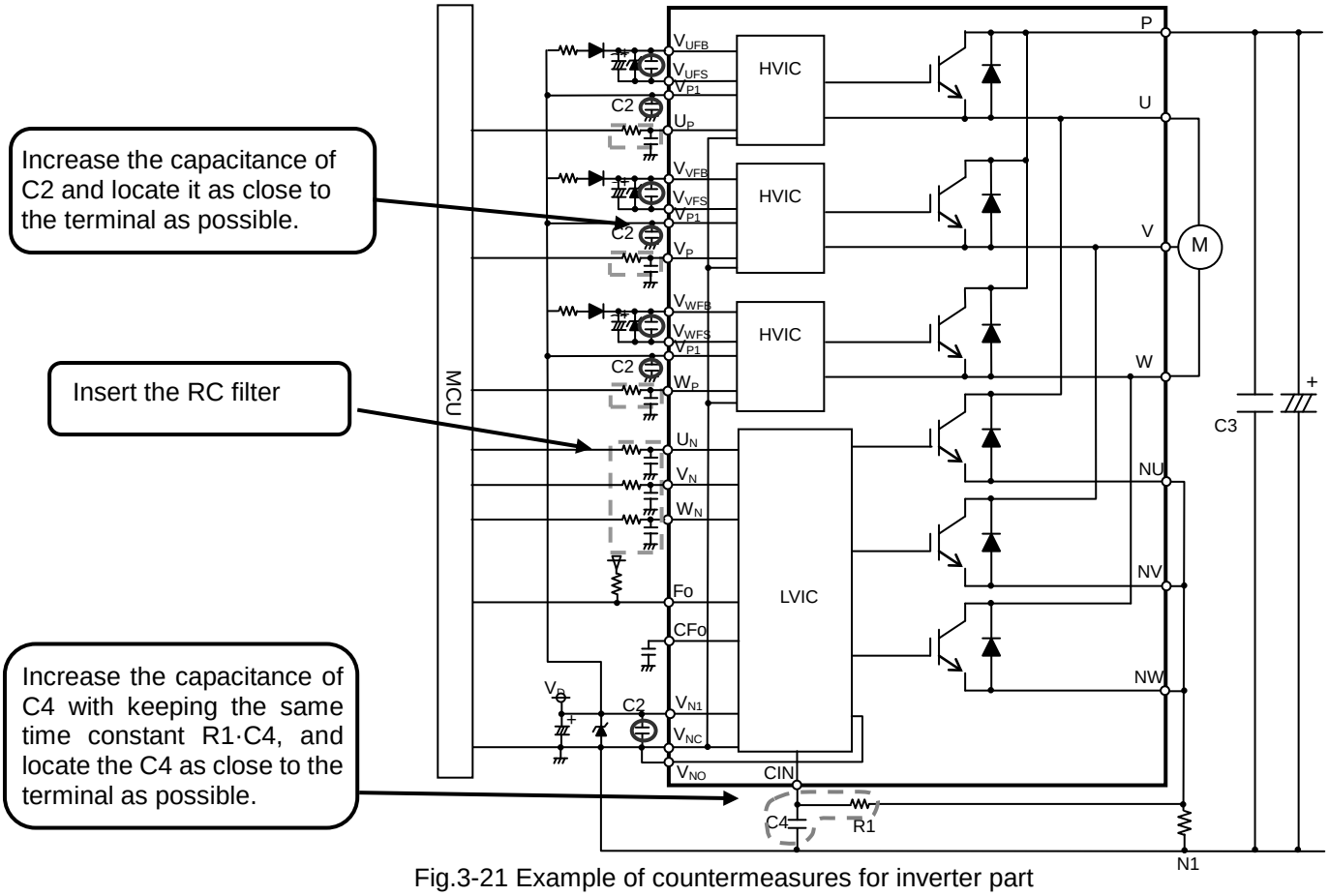


Fig.3-21 Example of countermeasures for inverter part

3.3.3 Static Electricity Withstand Capability

DIPIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-22, 23. The results (typical data) are described in Table 3-4.

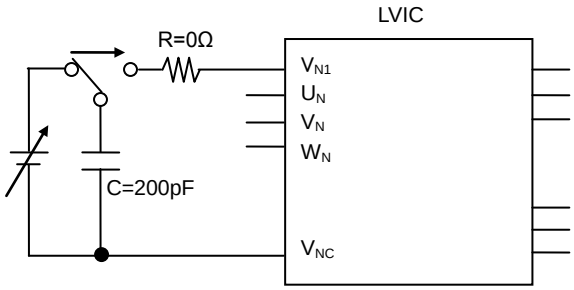


Fig.3-22 LVIC terminal Surge Test circuit

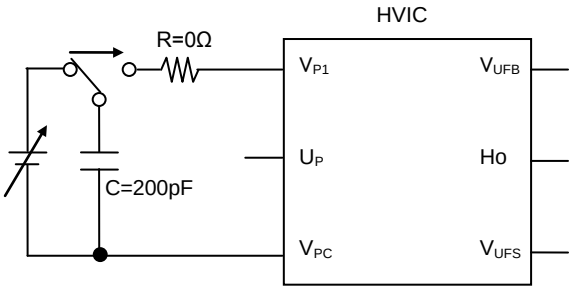


Fig.3-23 HVIC terminal Surge Test circuit

Conditions: Surge voltage increases in steps of 0.1V and only one-shot surge pulse is impressed at each voltage.
(Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-4 Typical ESD capability for PS219765, PS21767

[Control terminal part]

For control part, since both have same circuit in the control IC, they have same capability.

Terminals	+	-
UP, VP, WP-V_{NC}	0.9	1.8
V_{P1} - V_{NC}	1.5	1.6
V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	3.7	3.5
UN, VN, WN-V_{NC}	1.0	1.5
V_{N1}-V_{NC}	1.8	3.1
CIN-V_{NC}	1.1	1.6
Fo-V_{NC}	1.0	1.9
CFO-V_{NC}	0.3	0.7
V_{NO}-V_{NC}	2.0	3.1

[Power terminal part for PS21765]

Terminals	+	-
P-N	4.0 or more	4.0 or more
U-N, V-N, W-N	3.2	4.0 or more

[Power terminal part for PS21767]

Terminals	+	-
P-N	4.0 or more	4.0 or more
U-N, V-N, W-N	4.0 or more	4.0 or more

(Unit: kV)

CHAPTER 4 KEY PARAMETERS SELECTING GUIDANCE

4.1 Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)}/SC$$

where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum value of SC trip level should be set less than the IGBT minimum saturation current which is 2.0 times as large as the rated current. For example, the maximum SC trip level of PS21767 should be set to 2.0 x 30=60.0A. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PS21767, there is +/-0.05V dispersion in the spec of $V_{SC(ref)}$ as shown in Table 4-1.

Table 4-1 Specification for $V_{SC(ref)}$ (unit: V)

Condition	Min	Typ	Max
Specification at Tj=25°C, VD=15V	0.43	0.48	0.53

Then, the range of SC trip level can be calculated by the following expressions:

$R_{Shunt(min)}=V_{SC(ref)\ max}$ /SC(max)

$R_{Shunt(typ)}= R_{Shunt(min)}$ / 0.95* then SC(typ) = $V_{SC(ref)\ typ}$ / $R_{Shunt(typ)}$

$R_{Shunt(max)}= R_{Shunt(typ)}$ x 1.05* then SC(min)= $V_{SC(ref)\ min}$ / $R_{Shunt(max)}$

*)This is the case that shunt resistance dispersion is within +/-5%.

So the SC trip level range is described as Table 4-2.

Table 4-2 Operative SC Range (unit: A) (R_{Shunt}=8.8mΩ(min), 9.3mΩ(typ), 9.8mΩ(max)

Condition	min.	typ.	max.
at Tj=25°C	43.9	51.6	60.0

(e.g. 8.8mΩ ($R_{shunt(min)}$)= 0.53V (=$V_{SC(max)}$) / 60A(=SC(max))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

where Vsc : CIN terminal input voltage, Ic: peak current, τ : RC time constant.

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 4-3.

Table 4-3 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

t_{TOTAL}=t1+t2

4.2 Bootstrap Circuit Operation

4.2.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor.

It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC, limiting resistance and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

The circuit current characteristics in switching situation of P-side IGBT are described below.

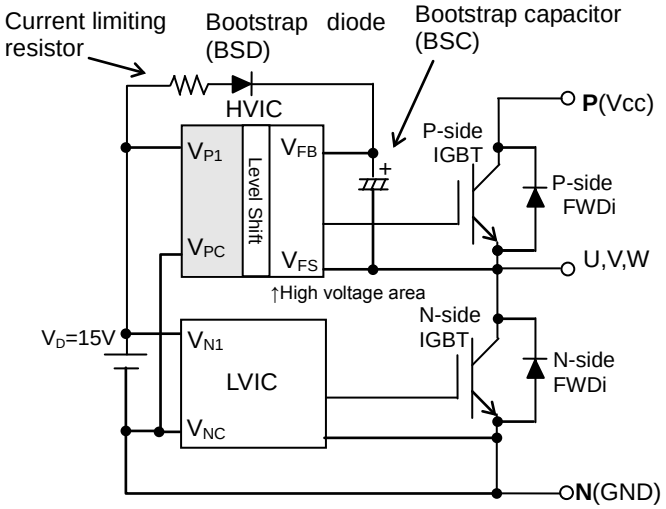


Fig.4-1 Bootstrap Circuit Diagram

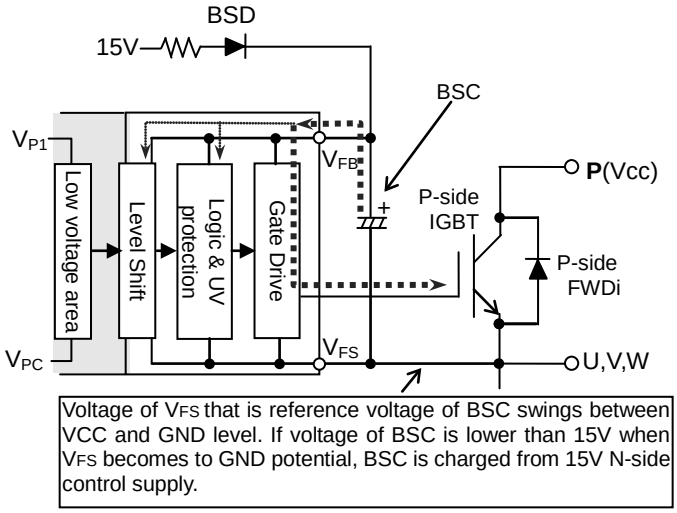


Fig.4-2 Bootstrap Circuit Diagram

4.2.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is max.0.55mA for PS2176* series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current will exceed 0.55mA and increases proportional to carrier frequency. For reference, Fig.4-3 to Fig.4-4 are the circuit current I_{DB} for P-side IGBT driving supply (V_{DB}) vs. carrier frequency characteristics. (@ V_D=V_{DB}=15V, Tj=125°C (largest I_{DB} temperature point), IGBT ON Duty=10, 30, 50, 70, 90%)

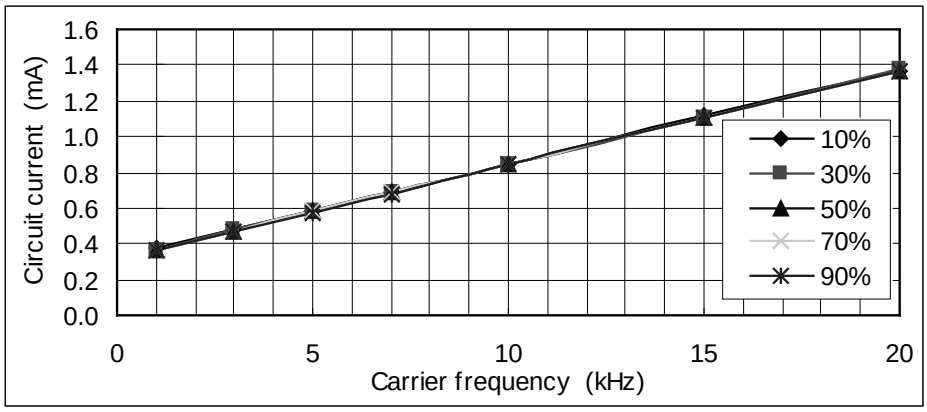


Fig.4-3 I_{DB} vs. Carrier frequency for PS21765

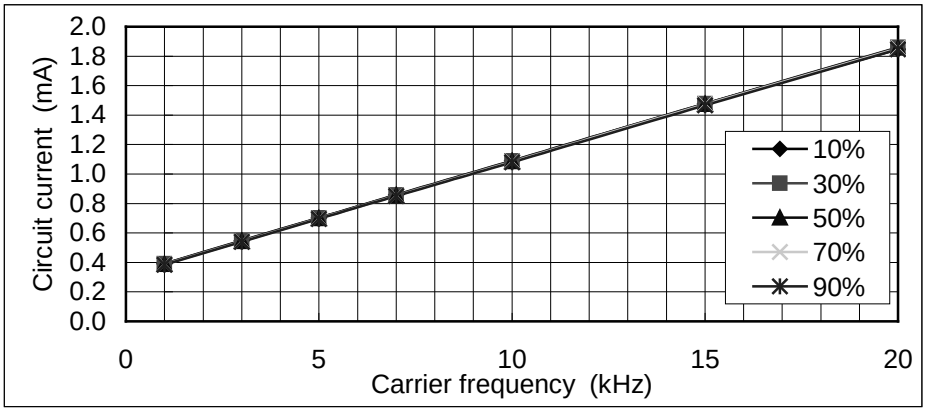


Fig.4-4 I_{DB} vs. Carrier frequency for PS21767

4.2.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-4.

Table 4-4 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	• Aluminum type: Low temp.: -10% High temp: +10% • Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on **-70%**~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

It is recommended for BSD to have same or higher blocking voltage with collector-emitter voltage V_{CES} of IGBT in DIPIPM. (i.e. 600V or more is needed in the case of 600V DIPIPM.) And its recovery time trr should be less than 100ns. (Fast recovery type)

Also ***it is highly recommended to apply the high quality product such as small variations of blocking voltage.*** If BSD broke by impressed overvoltage and shorted, it leads to the control ICs over voltage destruction because DC-link voltage (Vcc) is impressed upon low voltage area of control ICs. Then DIPIPM will lose various functions like protection and gate driving and it may lead to serious system destruction.

(3) Current limiting resistor

When designing limiting resistor, it is important to note its power rating, surge withstand capability (there is the possibility that surge may be impressed on the resistor when switching ON or OFF timing) and so on.
Especially if small chip type resistor is applied, it is recommended to select anti-surge designed type. For detailed information, please refer to the resistor manufacturer.

CHAPTER 5 Interface Demo Board

5.1 Mini DIPIPM Ver.4 Interface Demo Board

This chapter describes the interface demo board of Mini DIPIPM Ver.4 as a reference for the design of user application PCB with Mini DIPIPM Ver.4.

(1) Demo Board Outline

The demo board consists of the minimum necessary components such as snubber capacitor, bootstrap circuit elements of Mini DIPIPM Ver.4 interface shown in Fig.5-1.

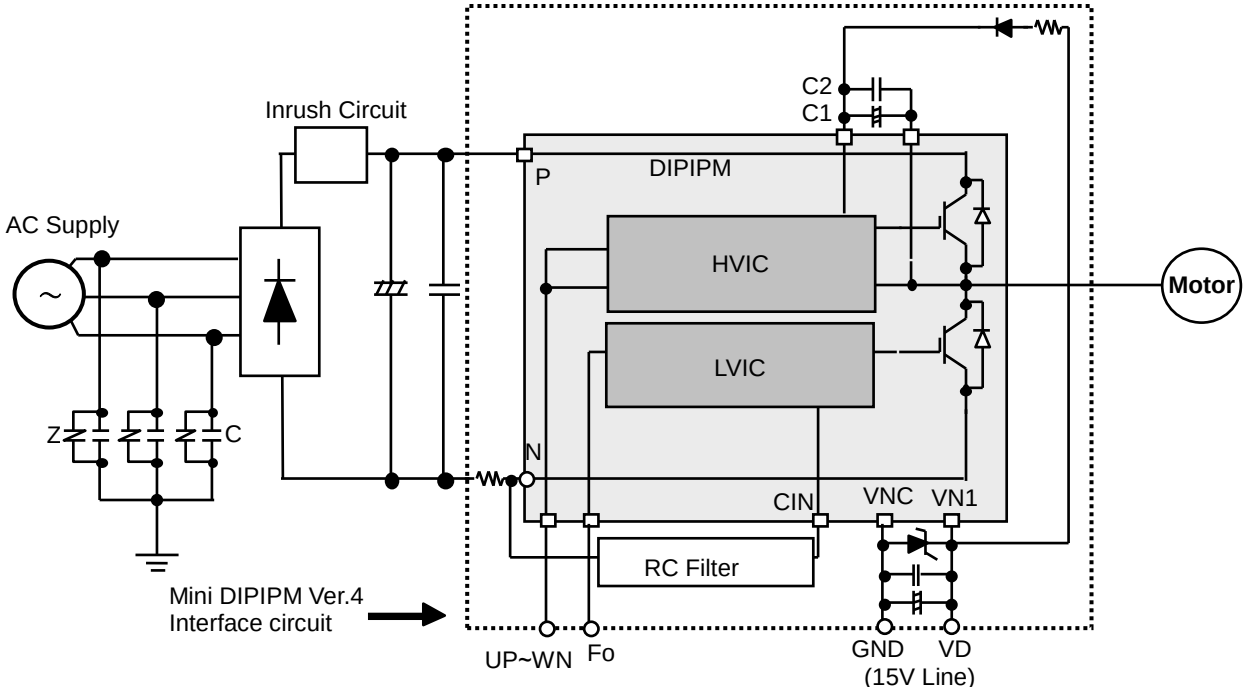
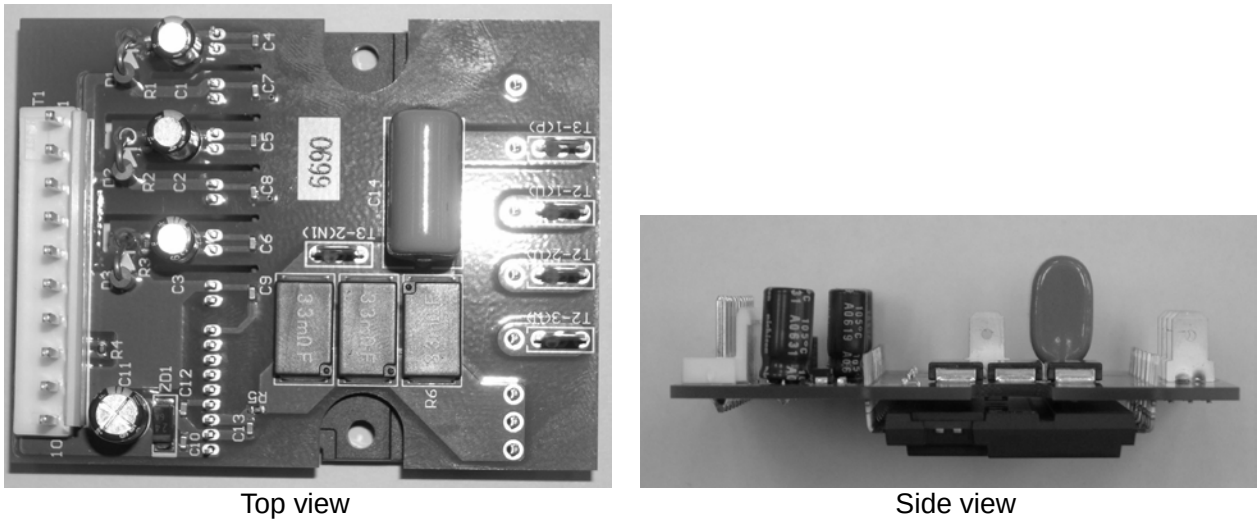


Fig.5-1 Demo board interface circuit

(2) Demo Board Photos



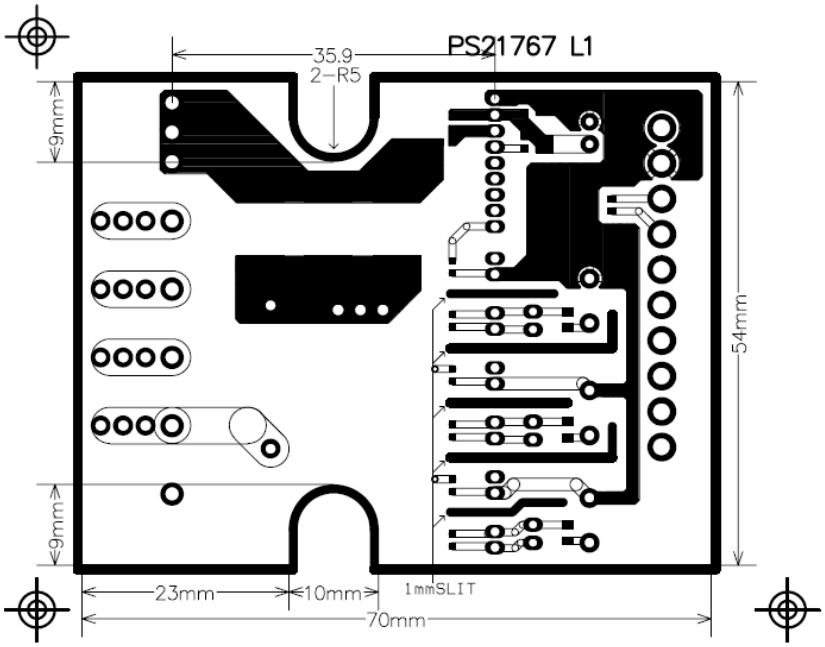
Top view　　Side view

Fig.5-2 Demo board photo

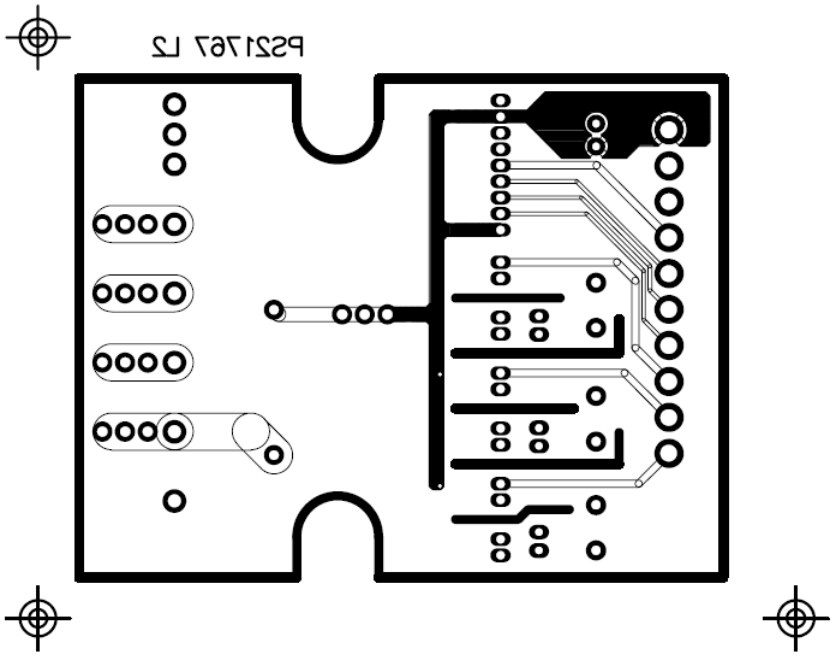
Note: Board dimension 70.0×54.0×24.2mm (including snubber capacitor height and module height)

5.2 Pattern Wiring

(1) PCB Pattern Layout



(a) Component side



(b) Solder side

Fig.5-3 Demo board PCB pattern layout

This evaluation board is made for your quick and temporary evaluation.
Please confirm and comply with your design standard when designing PCB pattern with reference to these patterns.

5.3 Circuit Schematic and Parts List

(1) Circuit Schematic

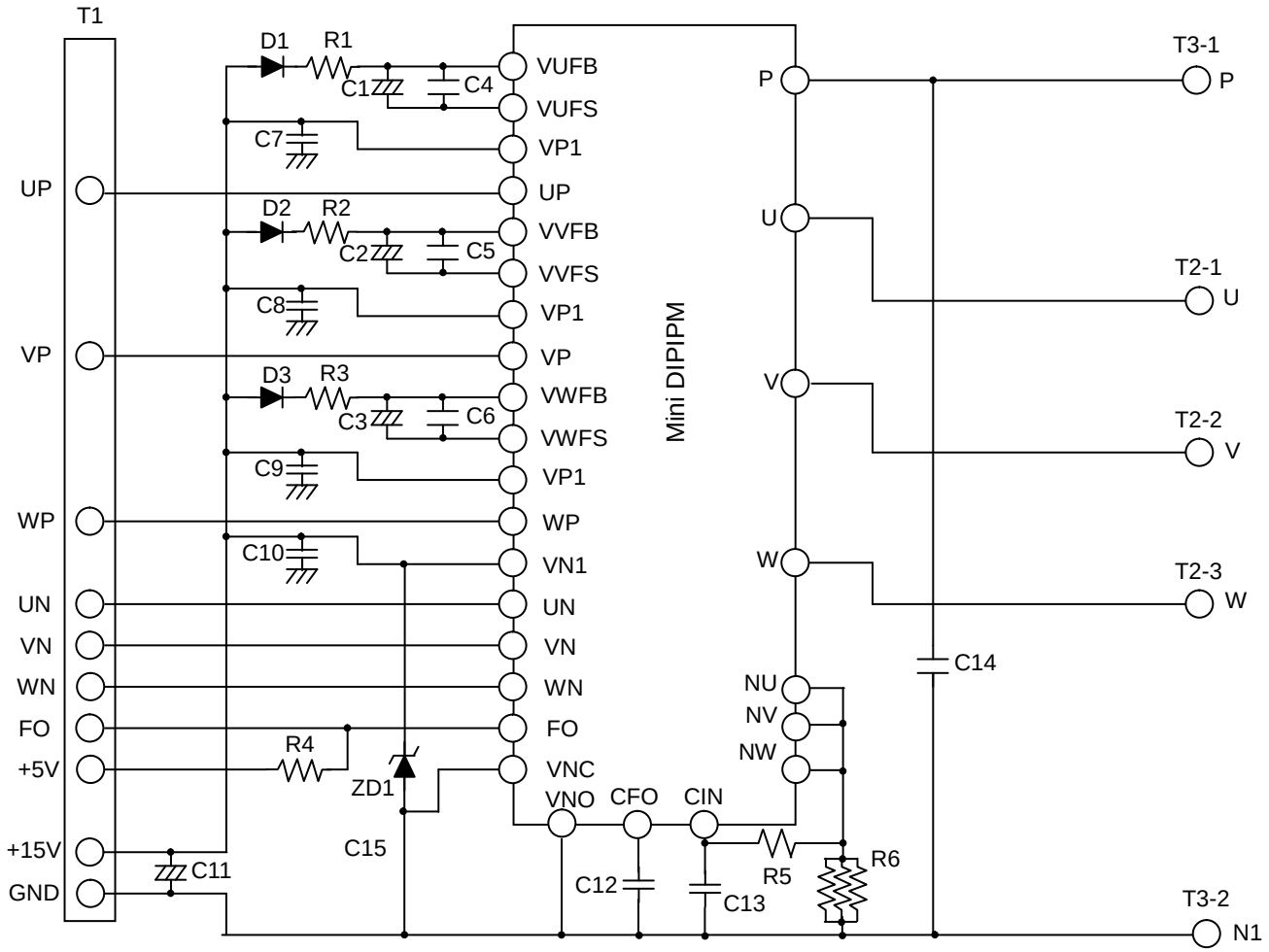


Fig.5-4 Demo board circuit schematic

Note: Although there is no zener diode mounted to P-side three floating drive supplies (between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}) on this demo board, it is highly recommend to add these zener diodes in actual system board.

(2) Parts List

Table 5-1 Parts list (only for reference)

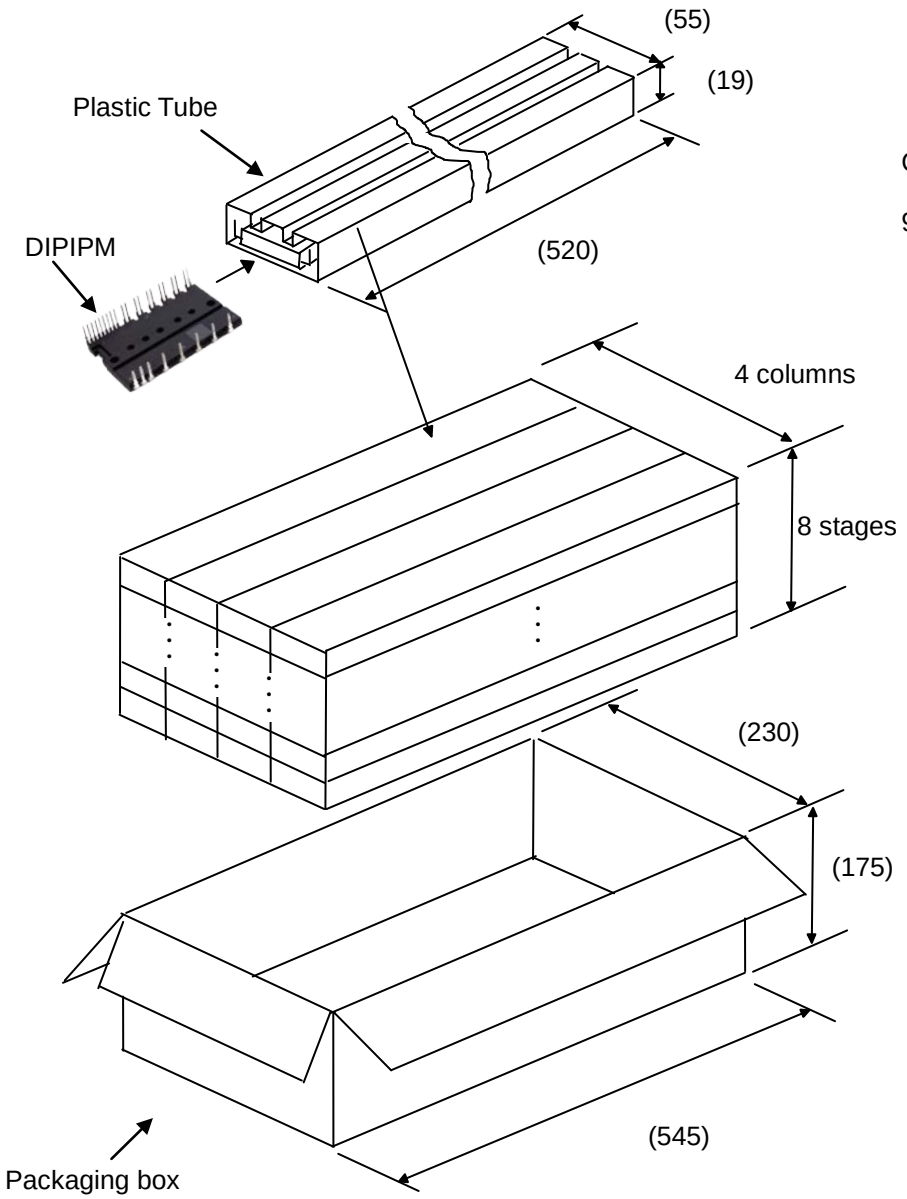
Symbol	Type Name	Description	Note
D1	10DRA60	1A 600V Diode	Japan International
D2	10DRA60	1A 600V Diode	Japan International
D3	10DRA60	1A 600V Diode	Japan International
ZD1	U1ZB24	24V 1W Zener Diode	Toshiba
C1	UPW1H220MDD	22μF50V Al electrolytic capacitor	Nichicon
C2	UPW1H220MDD	22μF50V Al electrolytic capacitor	Nichicon
C3	UPW1H220MDD	22μF50V Al electrolytic capacitor	Nichicon
C4	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C5	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C6	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C7	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C8	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C9	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C10	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C11	UPW1H470MED	47μF50V Al electrolytic capacitor	Nichicon
C12	GRM39R223K50	0.022μF50V ceramic capacitor	Murata
C13	C1608X7R1H102K	1000pF50V ceramic capacitor	TDK
C14	MDDSA0.22μF630	0.22μF630V snubber capacitor	Hitachi AIC
R1	RK73H1JTD10F	1/16W 10ΩF	Hokuriku Denko
R2	RK73H1JTD10F	1/16W 10Ω F	Hokuriku Denko
R3	RK73H1JTD10F	1/16W 10Ω F	Hokuriku Denko
R4	RK73H1JTD10kF	1/16W 10KΩ F	Hokuriku Denko
R5	RK73H1JTD2kF	1/16W 2KΩ F	Hokuriku Denko
R6-1	SL2TBK33/47LOF	PS21765: 47mΩ, ±1%, 2WX3 PS21767: 33mΩ, ±1%, 2WX3	KOA, Current detecting resistor
R6-2	SL2TBK33/47LOF		
R6-3	SL2TBK33/47LOF		
T1	B10P-VH	10pin Socket	JST
T2-1	TP42097-21	Faston* tab	Kyoushin
T2-2	TP42097-21	Faston* tab	Kyoushin
T2-3	TP42097-21	Faston* tab	Kyoushin
T3-1	TP42097-21	Faston* tab	Kyoushin
T3-2	TP42097-21	Faston* tab	Kyoushin

* Faston is the trademark of Tyco Electronics Corporation.

These are example of parts for this evaluation board.
When selecting parts for your PCB, please comply with your design standard and consider life time, reliability and so on.

CHAPTER 6 PACKAGE HANDLING

6.1 Packaging Specification



Quantity:

9pcs per 1 tube

Total amount in one box (max):

Tube Quantity: 4 × 8=32pcs
IPM Quantity: 32 × 9=288pcs

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):

About 21g per 1pcs of DIPIPM
About 300g per 1 tube
About 11kg per 1 box

Spacers are inserted into the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.6-1 Mini DIPIPM Ver.4 Packaging Specification

6.2 Handling Precautions

⚠ Cautions	
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.
Static electricity	・ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. *During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. (2)Notice when the control terminals are open *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.

Revision Record

Rev.	Date	Points
1	2011/6/15	New
2	2012/11/15	P.32 Fig.3-21 Example of countermeasures for inverter part P.35 Section 4.2 Bootstrap Circuit Operation

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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