

# DATA SHEET

**74LV251**

**8-input multiplexer (3-State)**

Product specification  
Supersedes data of 1997 Apr 10  
IC24 Data Handbook

1998 May 20

## 8-input multiplexer (3-State)

## 74LV251

## FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV251 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT251.

The 74LV251 is an 8-input multiplexer with 8 binary inputs ( $I_0$  to  $I_7$ ), an output enable input ( $\overline{OE}$ ) and three select inputs ( $S_0, S_1, S_2$ ). One of the eight binary inputs is selected by the select inputs and is routed to the outputs ( $\overline{Y}, Y$ ). Both outputs are in the high impedance OFF-state ( $Z$ ) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

## QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $I_n$ to $Y$ $I_n$ to $\overline{Y}$ $S_n$ to $Y$ $S_n$ to $\overline{Y}$	$C_L = 15$ pF; $V_{CC} = 3.3$ V	14 16 19 20	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	$V_{CC} = 3.3$ V $V_I = GND$ to $V_{CC}^1$	44	pF

## NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

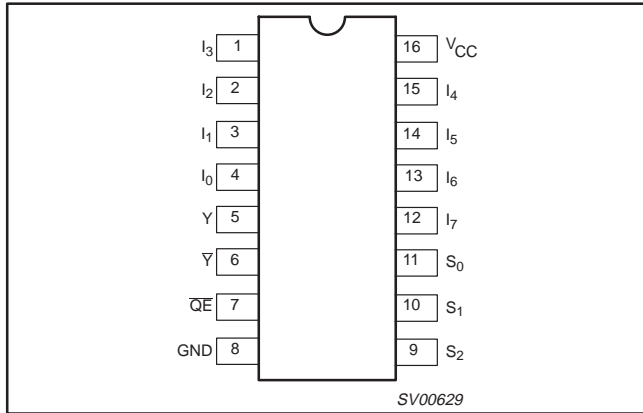
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV251 N	74LV251 N	SOT38-4
16-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV251 D	74LV251 D	SOT109-1
16-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV251 DB	74LV251 DB	SOT338-1
16-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV251 PW	74LV251PW DH	SOT403-1

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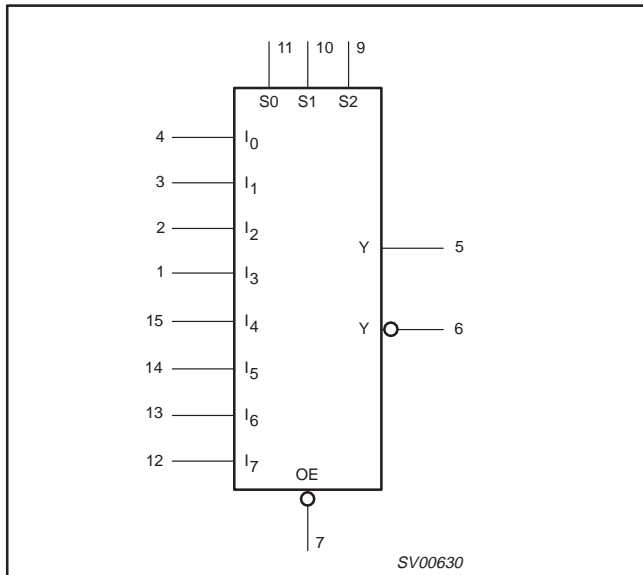
## PIN CONFIGURATION



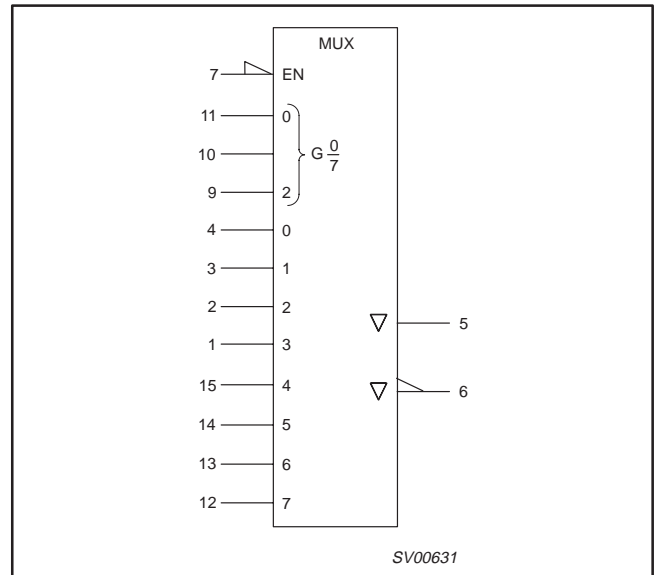
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I <sub>0</sub> to I <sub>7</sub>	Multiplexer inputs
5	Y	Multiplexer output
6	$\bar{Y}$	Complementary multiplexer output
7	$\overline{OE}$	3-State output enable input (active LOW)
8	GND	Ground (0 V)
11, 10, 9	S <sub>0</sub> to S <sub>2</sub>	Select inputs
16	V <sub>CC</sub>	Positive supply voltage

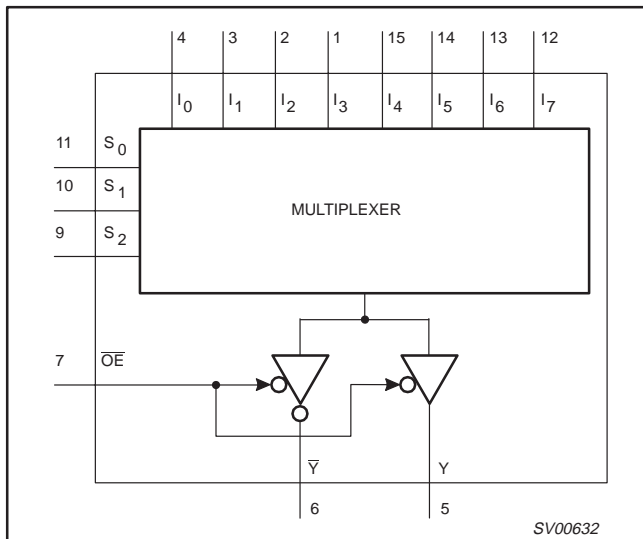
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## FUNCTIONAL DIAGRAM



## 8-input multiplexer (3-State)

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## FUNCTION TABLE

INPUTS												OUTPUTS	
OE	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	Y	Z
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

## NOTES:

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V <sub>I</sub>	Input voltage		0	–	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	–	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.0V to 2.0V V <sub>CC</sub> = 2.0V to 2.7V V <sub>CC</sub> = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

## NOTE:

1. The LV is guaranteed to function down to V<sub>CC</sub> = 1.0V (input levels GND or V<sub>CC</sub>); DC characteristics are guaranteed from V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 5.5V.

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$ , $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2 V$	0.9			0.9		V
		$V_{CC} = 2.0 V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6 V$	2.0			2.0		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2 V$			0.3		0.3	V
		$V_{CC} = 2.0 V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6 V$			0.8		0.8	
$V_{OH}$	HIGH level output voltage; all outputs	$V_{CC} = 1.2 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.8	3.0		2.8		
$V_{OH}$	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 6mA$	2.40	2.82		2.20		V
$V_{OL}$	LOW level output voltage; all outputs	$V_{CC} = 1.2 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0				V
		$V_{CC} = 2.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
$V_{OL}$	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 6mA$		0.25	0.40		0.50	V

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## DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	μA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		160	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V			500		850	μA

**NOTE:**

1. All typical values are measured at T<sub>amb</sub> = 25°C.

## AC CHARACTERISTICS

GND = 0V; t<sub>r</sub> = t<sub>f</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				V <sub>CC</sub> (V)	MIN	TYP <sup>1</sup>	MAX	MIN	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay I <sub>n</sub> to Y	Figure 1	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17 <sup>2</sup>	34		41	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay I <sub>n</sub> to $\bar{Y}$	Figure 2	1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19 <sup>2</sup>	38		45	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay S <sub>n</sub> to Y	Figure 1	1.2		120				ns
			2.0		41	77		92	
			2.7		30	56		68	
			3.0 to 3.6		23 <sup>2</sup>	45		54	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay S <sub>n</sub> to $\bar{Y}$	Figure 2	1.2		125				ns
			2.0		43	82		97	
			2.7		31	60		71	
			3.0 to 3.6		24 <sup>2</sup>	48		57	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output disable time OE to Y, $\bar{Y}$	Figure 2	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12 <sup>2</sup>	25		30	
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time OE to Y, $\bar{Y}$	Figure 2	1.2		60				ns
			2.0		22	39		48	
			2.7		17	29		36	
			3.0 to 3.6		13 <sup>2</sup>	24		29	

**NOTES:**

1. Unless otherwise stated, all typical values are measured at T<sub>amb</sub> = 25°C
2. Typical values are measured at V<sub>CC</sub> = 3.3 V.

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### AC WAVEFORMS

$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_M = 0.5 \text{ V} \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_X = V_{OL} + 0.1 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$   
 $V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_Y = V_{OH} - 0.1 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$

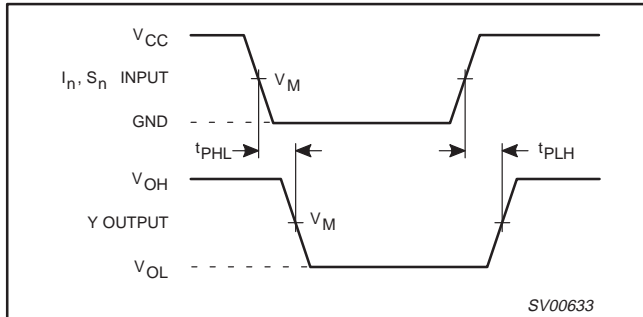


Figure 1. Multiplexer input ( $I_n$ ) and select input ( $S_n$ ) to output (Y) propagation delays.

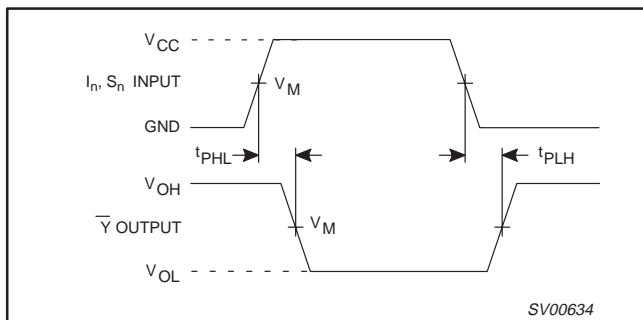


Figure 2. Multiplexer input ( $I_n$ ) and the select input ( $S_n$ ) to output ( $\bar{Y}$ ) propagation delays.

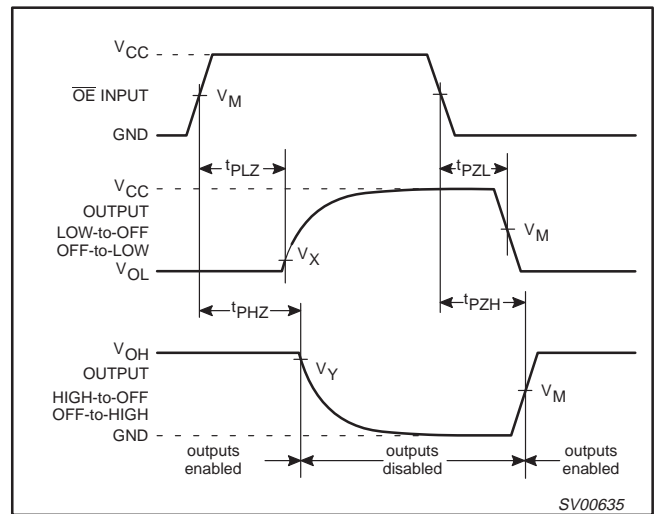


Figure 3. 3-State enable and disable times

### TEST CIRCUIT

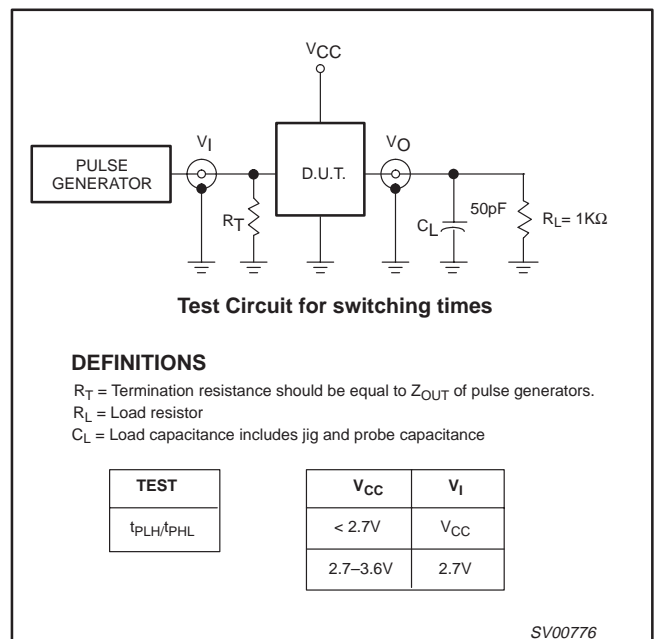


Figure 4. Load circuitry for switching times.

# 8-input multiplexer (3-State)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

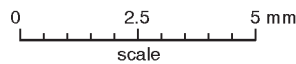
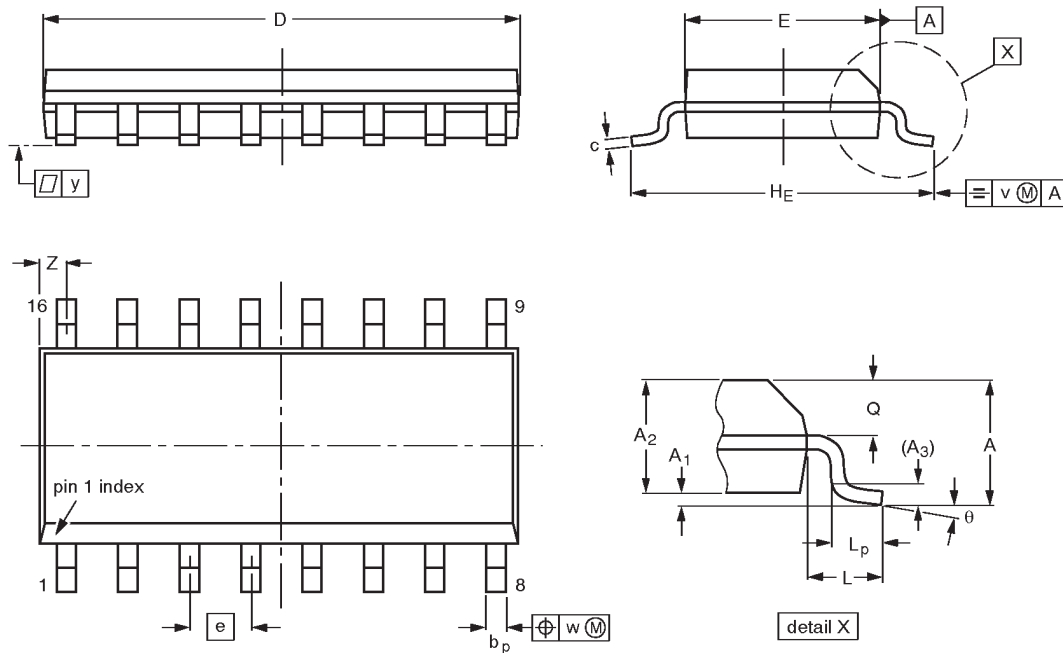


# 8-input multiplexer (3-State)

# 74LV251

**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

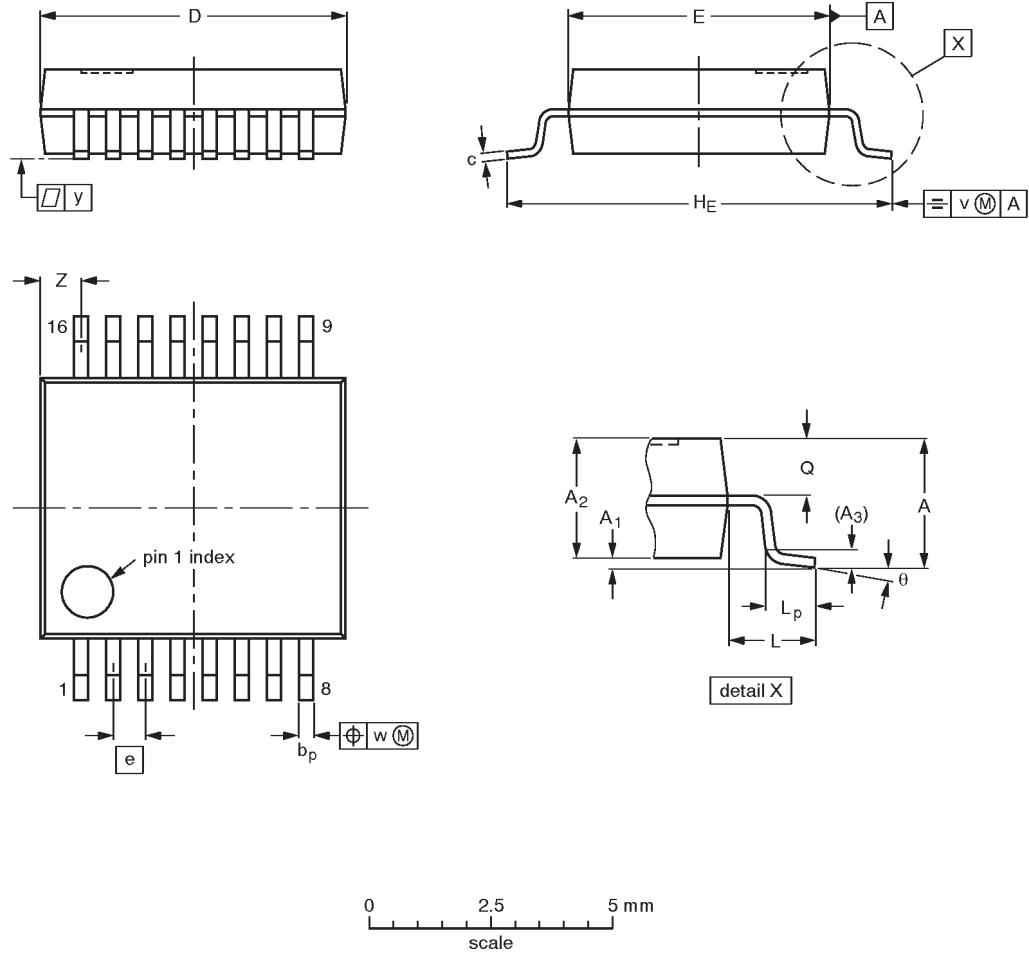
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

# 8-input multiplexer (3-State)

# 74LV251

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm**

**SOT338-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

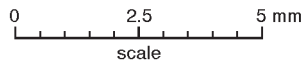
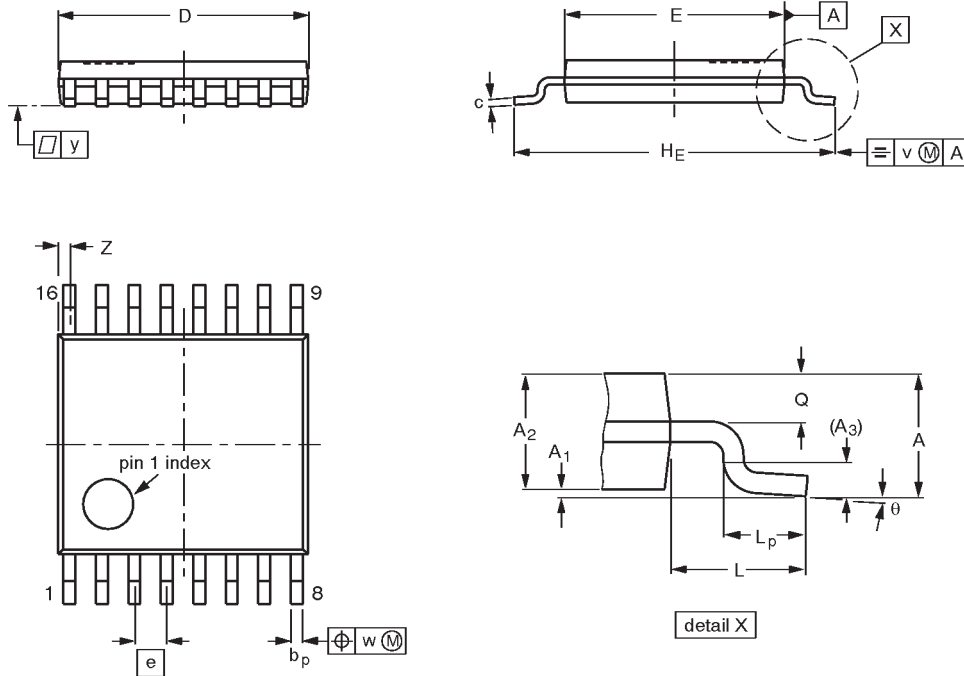
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

# 8-input multiplexer (3-State)

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**TSSOP16:** plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**SOT403-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

## 8-input multiplexer (3-State)

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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