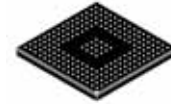


MPC5125



324 TEPBGA
23 mm x 23 mm

MPC5125 Microcontroller Data Sheet

The MPC5125 integrates a high performance e300 CPU core based on the Power Architecture® Technology with a rich set of peripheral functions focused on communications and systems integration.

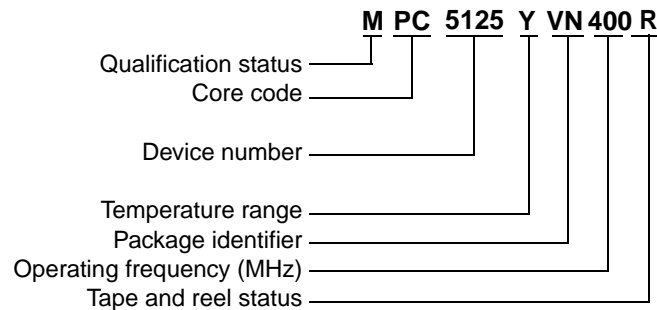
Major features of the MPC5125 are as follows:

- e300 Power Architecture processor core (enhanced version of the MPC603e core), operates as fast as 400 MHz
- Low power design
- Display interface unit (DIU)
- DDR1, DDR2, low-power mobile DDR (LPDDR), and 1.8 V/3.3 V SDR DRAM memory controllers
- 32 KB on-chip SRAM
- USB 2.0 OTG controller with ULPI interface
- DMA subsystem
- Flexible multi-function external memory bus (EMB) interface
- NAND flash controller (NFC)
- LocalPlus interface (LPC)
- 10/100Base Ethernet
- MMC/SD/SDIO card host controller (SDHC)
- Programmable serial controller (PSC)
- Inter-integrated circuit (I²C) communication interfaces
- Controller area network (CAN)
- J1850 byte data link controller (BDLC) interface
- On-chip real-time clock (RTC)
- On-chip temperature sensor
- IC Identification module (IIM)

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1 Ordering Information



Temperature Range
Y = -40 °C to 125 °C, junction

Package Identifier
VN = 324 TEPBGA Pb-free

Operating Frequency
400 = 400 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status

P = Pre qualification

M = Fully spec. qualified, general market flow

S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to [Table 1](#).

Figure 1. MPC5125 Orderable Part Number Description

[Table 1](#) shows the orderable part numbers for the MPC5125.

Table 1. MPC5125 Orderable Part Numbers

| Freescale Part Number ¹ | Package Description | Speed (MHz) | Operating Temperature ² | |
|------------------------------------|---|--------------------------------------|------------------------------------|-----------------------|
| | | Max ³ (f _{MAX}) | Min (T _L) | Max (T _H) |
| MPC5125YVN400 | MPC5125 324TEPBGA package Lead-free (PbFree) | 400 MHz core 200 MHz bus | -40 °C | 125 °C |

NOTES:

¹ All packaged devices are PPC5125, rather than MPC125, until product qualifications are complete.

² The lowest ambient operating temperature (T_A) is referenced by T_L; the highest junction temperature is referenced by T_H.

³ Maximum speed is the maximum frequency allowed including frequency modulation (FM).

2 MPC5125 Block Diagrams

Figure 2 shows a simplified MPC5125 block diagram.

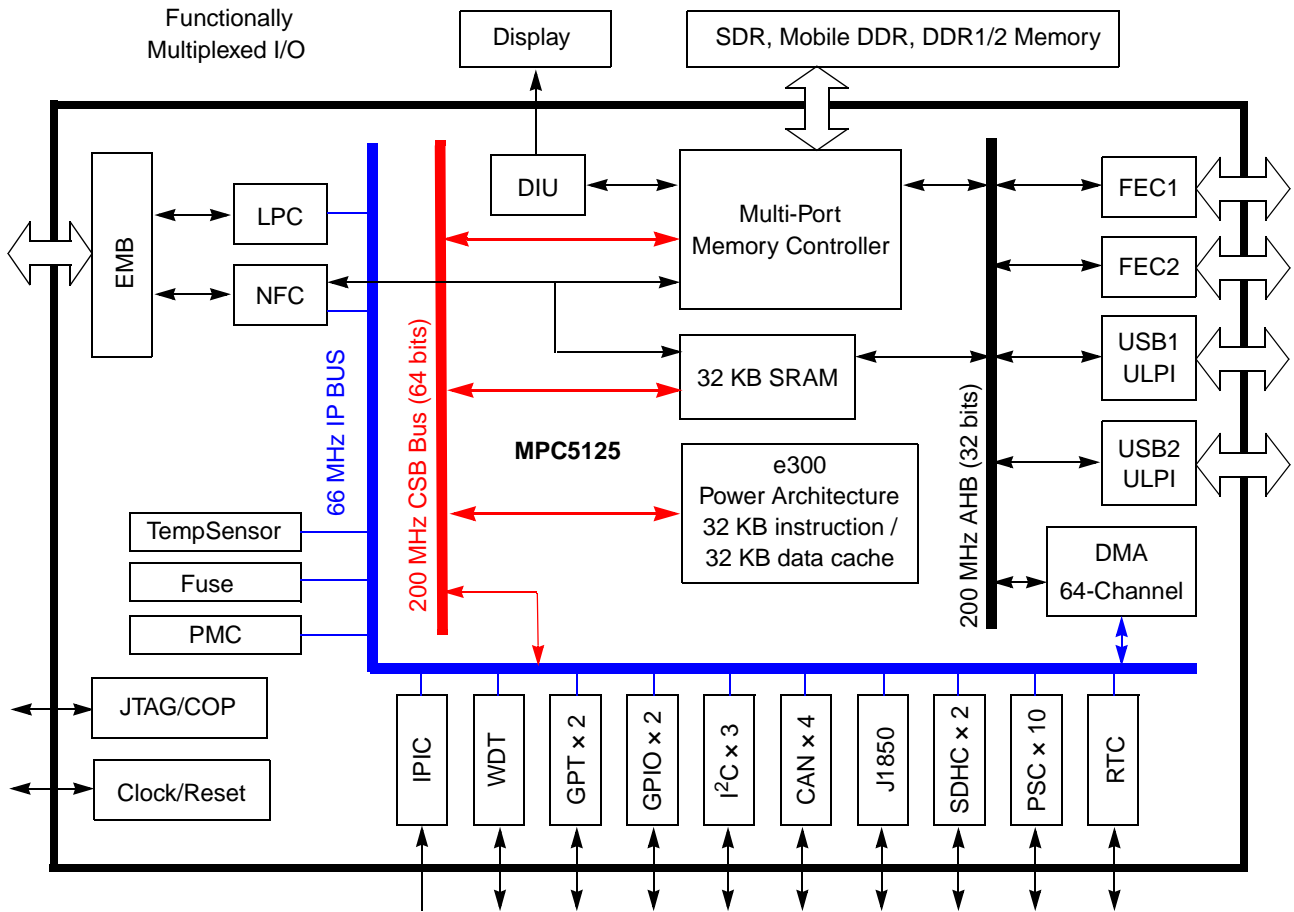


Figure 2. Simplified MPC5125 Block Diagram

3 Pin Assignments

This section details pin assignments.

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments.

| | | | | | | | | | | | | | | | | | | | | | | | |
|----|-------------|------------|------------|-------------|------------|--------------|------------|-------------|--------------|----------------------|------------|-----------|-----------|-----------|-----------|-----------|-------------|-----------|-------------|-------------|-------------|-------------|-------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | |
| A | VSS | VSS | EMB_A D01 | EMB_A D00 | GPIO01 | GPIO02 | RTC_X TALO | RTC_X TALI | SYS_X TALI | SYS_X TALO | AVDD_SPLL | PSC0_1 | PSC0_2 | VDD_I O | PSC1_4 | CAN2_TX | HRESET_B | SRESET_B | I2C1_S DA | MCAS_B | MWE_B | VSS | |
| B | VSS | EMB_A D05 | EMB_A D03 | EMB_A D02 | J1850_TX | GPIO00 | VSS | CAN2_RX | VDD_I O | AVSS_OSC_T MPS_S PLL | AVSS_CPLL | VDD_I O | PSC0_3 | PSC1_2 | CAN1_TX | TDO | VDD_I O | I2C1_S CL | VDD_I O_MEM | MA15 | MA14 | MA11 | |
| C | EMB_A D11 | EMB_A D09 | EMB_A D07 | EMB_A D06 | VDD_I O | J1850_RX | GPIO03 | HIB_M ODE_B | CAN1_RX | AVDD_OSC_T MPS | PSC0_0 | PSC1_0 | PSC1_1 | VDD_I O | TDI | TCK | PORESET_B | MCKE | MRAS_B | MA12 | VDD_I O_MEM | MA09 | |
| D | TMPS_ANAVIZ | EMB_A D10 | VDD_I O | AVDD_FUSEWR | EMB_A D04 | PSC_M CLK_IN | VSS | VBAT | SPLL_A NAVIZ | AVDD_CPLL | PSC0_4 | VSS | PSC1_3 | TEST | TMS | TRST_B | VDD_I O_MEM | MCS_B | VDD_I O_MEM | MA13 | MA08 | MA06 | |
| E | EMB_A D15 | EMB_A D13 | EMB_A D12 | EMB_A D08 | | | | | | | | | | | | | | | | MA10 | MA07 | MA04 | MA03 |
| F | EMB_A D21 | VDD_I O | EMB_A D16 | VSS | | | | | | | | | | | | | | | | MA02 | MA05 | VSS | MA01 |
| G | EMB_A D25 | EMB_A D18 | EMB_A D17 | VDD_I O | | | | | | | | | | | | | | | | VDD_I O_MEM | MA00 | MBA2 | MCK_B |
| H | EMB_A D28 | VDD_I O | EMB_A D20 | EMB_A D14 | | | | | | | | | | | | | | | | MBA0 | MBA1 | VDD_I O_MEM | MCK |
| J | EMB_A D31 | EMB_A D26 | EMB_A D23 | EMB_A D19 | | | | | VSS | VDD | VDD | VDD | VDD | VSS | | | | | | MODT | MDQ31 | MDQ30 | MDQ29 |
| K | EMB_A X00 | VSS | EMB_A D24 | EMB_A D22 | | | | | VSS | VSS | VSS | VSS | VSS | VDD | | | | | | MVTT3 | MDQ28 | VSS | MDM3 |
| L | LPC_A X03 | EMB_A X02 | EMB_A D29 | VSS | | | | | VDD | VSS | VSS | VSS | VSS | VDD | | | | | | VSS | MDQ26 | MDQ27 | MDQ25 |
| M | LPC_C S0_B | VDD_I O | EMB_A D30 | EMB_A D27 | | | | | VDD | VSS | VSS | VSS | VSS | VDD | | | | | | MVTT2 | MDQ23 | MDQ24 | MDQ25 |
| N | NFC_R B | LPC_O E_B | LPC_R WB | EMB_A X01 | | | | | VSS | VSS | VSS | VSS | VSS | VDD | | | | | | MVREF | MDQ20 | VSS | MDQ22 |
| P | NFC_C E0_B | VSS | LPC_A CK_B | VSS | | | | | VSS | VDD | VDD | VDD | VDD | VSS | | | | | | VDD_I O_MEM | MDQ18 | MDQ21 | MDQ21 |
| R | SDHC1_D2 | SDHC1_D3 | VDD_I O | LPC_C LK | | | | | | | | | | | | | | | | MVTT1 | MDQ16 | VDD_I O_MEM | MDM2 |
| T | SDHC1_CLK | SDHC1_CMD | SDHC1_D0 | SDHC1_D1 | | | | | | | | | | | | | | | | VDD_I O_MEM | MDQ13 | MDQ17 | MDQ19 |
| U | FEC1_CRS | VSS | FEC1_COL | I2C2_S DA | | | | | | | | | | | | | | | | MDQ07 | MDQS1 | VSS | MDQ15 |
| V | FEC1_MDC | FEC1_MDIO | VDD_I O | I2C2_S CL | | | | | | | | | | | | | | | | VDD_I O_MEM | MDQ10 | MDM1 | MDQ14 |
| W | FEC1_TX_CLK | FEC1_TX_ER | FEC1_TXD_1 | FEC1_TXD_0 | VDD_I O | USB1_STOP | USB1_DIR | VSS | USB1_DATA1 | VSS | DIU_HS YNC | VSS | DIU_LD_08 | DIU_LD_13 | VDD_I O | DIU_LD_21 | VSS | MVTT0 | VDD_I O_MEM | MDQ06 | MDQ11 | MDQ12 | |
| Y | FEC1_TXD_3 | VSS | FEC1_TX_EN | FEC1_RXD_2 | FEC1_RX_ER | USB1_DATA6 | USB1_DATA5 | USB1_CLK | USB1_DATA0 | DIU_LD_01 | DIU_LD_03 | DIU_LD_07 | DIU_LD_10 | DIU_LD_14 | DIU_LD_17 | DIU_LD_22 | DIU_VS YNC | MDQ01 | MDM0 | MDQ05 | VDD_I O_MEM | MDQ09 | |
| AA | FEC1_TXD_2 | FEC1_RXD_3 | FEC1_RXD_1 | VDD_I O | USB1_NEXT | VSS | USB1_DATA4 | DIU_DE | VDD_I O | DIU_LD_02 | DIU_LD_04 | VDD_I O | DIU_LD_11 | VDD_I O | DIU_LD_16 | VDD_I O | DIU_LD_23 | VSS | MDQ02 | MDQS0 | MDQ04 | MDQ08 | |
| AB | VSS | FEC1_RXD_0 | FEC1_RX_DV | FEC1_RX_CLK | USB1_DATA7 | USB1_DATA3 | USB1_DATA2 | DIU_CLK | DIU_LD_00 | DIU_LD_05 | DIU_LD_06 | DIU_LD_09 | DIU_LD_12 | DIU_LD_15 | DIU_LD_18 | DIU_LD_19 | DIU_LD_20 | VDD_I O | MDQ00 | VDD_I O_MEM | MDQ03 | VSS | |

Figure 3. Ball Map for the MPC5125 324 TEPBGA Package

3.2 Pin Muxing and Reset States

Table 2 provides the pinout listing for the MPC5125.

Table 2. MPC5125 Pin Multiplexing

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-----------------------|---|---------------------------------|--------------------------|-------------------------|------------------|--------------|---|-----|
| GPIO00 | — | ALT0 ALT1 ALT2 ALT3 | GPIO00 — — — | GPIO1 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | B6 |
| GPIO01 | — | ALT0 ALT1 ALT2 ALT3 | GPIO01 — — — | GPIO1 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | A5 |
| GPIO02 | — | ALT0 ALT1 ALT2 ALT3 | GPIO02 — — — | GPIO1 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | A6 |
| GPIO03 | — | ALT0 ALT1 ALT2 ALT3 | GPIO03 — — — | GPIO1 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | C7 |
| RTC_XTALI | — | ALT0 ALT1 ALT2 ALT3 | RTC_XTALI — — — | RTC — — — | I — — — | VBAT | — | A8 |
| RTC_XTALO | — | ALT0 ALT1 ALT2 ALT3 | RTC_XTALO — — — | RTC — — — | O — — — | VBAT | — | A7 |
| HIB_MODE | — | ALT0 ALT1 ALT2 ALT3 | HIB_MODE — — — | RTC — — — | O — — — | VBAT | In Hibernation mode , this pin provides a signal to shut down an external power supply. | C8 |
| Analog Visible Signal | | | | | | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|--------------------------|---|---------------------------------|---|-------------------------|------------------|------------------|-------|-----|
| SPLL_ANAVIZ | — | ALT0 ALT1 ALT2 ALT3 | SPLL_ANAVIZ — — — | — — — — | — — — — | — | — | D9 |
| TMPS_ANAVIZ | — | ALT0 ALT1 ALT2 ALT3 | TMPS_ANAVIZ — — — | — — — — | — — — — | — | — | D1 |
| SYS_XTALI | — | ALT0 ALT1 ALT2 ALT3 | SYS_XTALI — — — | SysClock — — — | I — — — | SYS_PLL _AVDD | — | A9 |
| SYS_XTALO | — | ALT0 ALT1 ALT2 ALT3 | SYS_XTALO — — — | SysClock — — — | O — — — | SYS_PLL _AVDD | — | A10 |
| $\overline{\text{MCS}}$ | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{MCS0}}$ — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | D18 |
| $\overline{\text{MCAS}}$ | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{MCAS}}$ — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | A20 |
| $\overline{\text{MRAS}}$ | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{MRAS}}$ — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | C19 |
| MVREF | — | ALT0 ALT1 ALT2 ALT3 | MVREF — — — | DRAM — — — | I — — — | VDD_IO_MEM | — | N19 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------------------------|---|---------------------------------|--|-------------------------|--------------------|--------------|-------|------|
| MVTT0 | — | ALT0 ALT1 ALT2 ALT3 | MVTT0 — — — | DRAM — — — | I — — — | VDD_IO_MEM | — | W18 |
| MVTT1 | — | ALT0 ALT1 ALT2 ALT3 | MVTT1 — — — | DRAM — — — | I — — — | VDD_IO_MEM | — | R19 |
| MVTT2 | — | ALT0 ALT1 ALT2 ALT3 | MVTT2 — — — | DRAM — — — | I — — — | VDD_IO_MEM | — | M19 |
| MVTT3 | — | ALT0 ALT1 ALT2 ALT3 | MVTT3 — — — | DRAM — — — | I — — — | VDD_IO_MEM | — | K19 |
| $\overline{\text{MWE}}$ | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{MWE}}$ — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | A21 |
| MDQ00 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ00 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | AB19 |
| MDQ01 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ01 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | Y18 |
| MDQ02 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ02 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | AA19 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------|---|---------------------------------|------------------------|-------------------------|--------------------|--------------|-------|------|
| MDQ03 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ03 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | AB21 |
| MDQ04 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ04 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | AA21 |
| MDQ05 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ05 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | Y20 |
| MDQ06 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ06 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | W20 |
| MDQ07 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ07 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | U19 |
| MDQ08 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ08 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | AA22 |
| MDQ09 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ09 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | Y22 |
| MDQ10 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ10 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | V20 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------|---|---------------------------------|----------------------------|-------------------------|----------------------|--------------|-------|-----|
| MDQ11 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ11 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | W21 |
| MDQ12 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ12 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | W22 |
| MDQ13 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ13 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | T20 |
| MDQ14 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ14 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | V22 |
| MDQ15 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ15 — — — | DRAM — — — | I/O — — — | VDD_IO_MEM | — | U22 |
| MDQ16 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ16 — — GPT1[0] | DRAM — — GPT1 | I/O — — I/O | VDD_IO_MEM | — | R20 |
| MDQ17 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ17 — — GPT1[1] | DRAM — — GPT1 | I/O — — I/O | VDD_IO_MEM | — | T21 |
| MDQ18 | 0x00 IO_CON- TROL_MEM | ALT0 ALT1 ALT2 ALT3 | MDQ18 — — GPT1[2] | DRAM — — GPT1 | I/O — — I/O | VDD_IO_MEM | — | P20 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------|---|---------------------------------|------------------------|-------------------------|---------------|--------------|-------|-----|
| MDQ19 | 0x00 | ALT0 | MDQ19 | DRAM | I/O | VDD_IO_MEM | — | T22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPT1[3] | — — GPT1 | — — I/O | | | |
| MDQ20 | 0x00 | ALT0 | MDQ20 | DRAM | I/O | VDD_IO_MEM | — | N20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPT1[4] | — — GPT1 | — — I/O | | | |
| MDQ21 | 0x00 | ALT0 | MDQ21 | DRAM | I/O | VDD_IO_MEM | — | P22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPT1[5] | — — GPT1 | — — I/O | | | |
| MDQ22 | 0x00 | ALT0 | MDQ22 | DRAM | I/O | VDD_IO_MEM | — | N22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPT1[6] | — — GPT1 | — — I/O | | | |
| MDQ23 | 0x00 | ALT0 | MDQ23 | DRAM | I/O | VDD_IO_MEM | — | M20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPT1[7] | — — GPT1 | — — I/O | | | |
| MDQ24 | 0x00 | ALT0 | MDQ24 | DRAM | I/O | VDD_IO_MEM | — | M21 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO21 | — — GPIO1 | — — I/O | | | |
| MDQ25 | 0x00 | ALT0 | MDQ25 | DRAM | I/O | VDD_IO_MEM | — | M22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO22 | — — GPIO1 | — — I/O | | | |
| MDQ26 | 0x00 | ALT0 | MDQ26 | DRAM | I/O | VDD_IO_MEM | — | L20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO23 | — — GPIO1 | — — I/O | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------|---|---------------------------------|------------------------|-------------------------|---------------|--------------|-------|-----|
| MDQ27 | 0x00 IO_CONTROL_MEM | ALT0 | MDQ27 | DRAM | I/O | VDD_IO_MEM | — | L21 |
| | | ALT1 | — | — | — | | | |
| MDQ28 | 0x00 IO_CONTROL_MEM | ALT2 | — | — | — | VDD_IO_MEM | — | K20 |
| | | ALT3 | GPIO24 | GPIO1 | I/O | | | |
| MDQ29 | 0x00 IO_CONTROL_MEM | ALT0 | MDQ29 | DRAM | I/O | VDD_IO_MEM | — | J22 |
| | | ALT1 | — | — | — | | | |
| MDQ30 | 0x00 IO_CONTROL_MEM | ALT2 | — | — | — | VDD_IO_MEM | — | J21 |
| | | ALT3 | GPIO27 | GPIO1 | I/O | | | |
| MDQ31 | 0x00 IO_CONTROL_MEM | ALT0 | MDQ31 | DRAM | I/O | VDD_IO_MEM | — | J20 |
| | | ALT1 | — | — | — | | | |
| MDM0 | 0x00 IO_CONTROL_MEM | ALT2 | — | — | — | VDD_IO_MEM | — | Y19 |
| | | ALT3 | GPIO28 | GPIO1 | I/O | | | |
| MDM1 | 0x00 IO_CONTROL_MEM | ALT0 | MDM0 | DRAM | O | VDD_IO_MEM | — | V21 |
| | | ALT1 | — | — | — | | | |
| MDM2 | 0x00 IO_CONTROL_MEM | ALT2 | — | — | — | VDD_IO_MEM | — | R22 |
| | | ALT3 | GPIO29 | GPIO1 | I/O | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------|---|---------------------------------|------------------------|-------------------------|---------------|--------------|-------|------|
| MDM3 | 0x00 | ALT0 | MDM3 | DRAM | O | VDD_IO_MEM | — | K22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO30 | — — GPIO1 | — — I/O | | | |
| MDQS0 | 0x00 | ALT0 | MDQS0 | DRAM | I/O | VDD_IO_MEM | — | AA20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |
| MDQS1 | 0x00 | ALT0 | MDQS1 | DRAM | I/O | VDD_IO_MEM | — | U20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |
| MDQS2 | 0x00 | ALT0 | MDQS2 | DRAM | I/O | VDD_IO_MEM | — | P21 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO31 | — — GPIO1 | — — I/O | | | |
| MDQS3 | 0x00 | ALT0 | MDQS3 | DRAM | I/O | VDD_IO_MEM | — | L22 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — GPIO32 | — — GPIO2 | — — I/O | | | |
| MBA0 | 0x00 | ALT0 | MBA0 | DRAM | O | VDD_IO_MEM | — | H19 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |
| MBA1 | 0x00 | ALT0 | MBA1 | DRAM | O | VDD_IO_MEM | — | H20 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |
| MBA2 | 0x00 | ALT0 | MBA2 | DRAM | O | VDD_IO_MEM | — | G21 |
| | IO_CONTROL_MEM | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------|---|---------------------------------|------------------------|-------------------------|------------------|--------------|-------|-----|
| MA00 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA00 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | G20 |
| MA01 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA01 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | F22 |
| MA02 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA02 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | F19 |
| MA03 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA03 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | E22 |
| MA04 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA04 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | E21 |
| MA05 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA05 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | F20 |
| MA06 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA06 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | D22 |
| MA07 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA07 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | E20 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------|---|---------------------------------|--------------------------|-------------------------|------------------|--------------|-------|-----|
| MA08 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA08 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | D21 |
| MA09 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA09 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | C22 |
| MA10 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA10 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | E19 |
| MA11 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA11 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | B22 |
| MA12 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA12 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | C20 |
| MA13 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA13 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | D20 |
| MA14 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA14 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | B21 |
| MA15 | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MA15/MCS1 — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | B20 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------------------------|---|---------------------------------|--|---------------------------|----------------------|--------------|-------|-----|
| MCK | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MCK — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | H22 |
| $\overline{\text{MCK}}$ | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MCK — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | G22 |
| MCKE | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MCKE — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | C18 |
| MODT | 0x00 IO_CONTROL_MEM | ALT0 ALT1 ALT2 ALT3 | MODT — — — | DRAM — — — | O — — — | VDD_IO_MEM | — | J19 |
| LPC_CLK | 0x04 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_CLK TPA1 — GPIO04 | LPC — — GPIO1 | O — — I/O | VDD_IO | — | R4 |
| LPC_OE_B | 0x05 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_OE PSC3_3 — GPIO05 | LPC PSC3 — GPIO1 | O I/O — I/O | VDD_IO | — | N2 |
| LPC_RWB | 0x06 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_R $\overline{\text{W}}$ PSC3_4 — GPIO06 | LPC PSC3 — GPIO1 | O I/O — I/O | VDD_IO | — | N3 |
| LPC_CS0_B | 0x07 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_CS0 — — GPIO07 | LPC — — GPIO1 | O — — I/O | VDD_IO | — | M1 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-----------|---|---------------------------------|---|----------------------------|----------------------|--------------|--|-----|
| LPC_ACK_B | 0x08 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_ACK/LPC_BURST NFC_CE1 LPC_CS1 GPIO08 | LPC NFC LPC GPIO1 | I/O O O I/O | VDD_IO | — | P3 |
| LPC_AX03 | 0x09 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AX03/LPC_TS NFC_CE2 LPC_CS2 — | LPC NFC LPC — | O O O — | VDD_IO | — | L1 |
| EMB_AD00 | 0x2C STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD00/NFC_AD00 — RST_CONF_LOC0 — | LPC — — — | I/O — — — | VDD_IO | ALT2: Reset configuration Boot ROM Location 0 | A4 |
| EMB_AD01 | 0x2B STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD01/NFC_AD01 — RST_CONF_LOC1 — | LPC — — — | I/O — — — | VDD_IO | ALT2: Reset configuration Boot ROM Location 1 | A3 |
| EMB_AD02 | 0x2A STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD02/NFC_AD02 — RST_CONF_BMS — | LPC — — — | I/O — — — | VDD_IO | ALT2: Reset configuration Boot Mode Select | B4 |
| EMB_AD03 | 0x29 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD03/NFC_AD03 — RST_CONF_LPCDBW0 — | LPC — — — | I/O — — — | VDD_IO | ALT2: Reset configuration LPC Port Size 0 | B3 |
| EMB_AD04 | 0x28 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD04/NFC_AD04 — RST_CONF_LPCDBW1 — | LPC — — — | I/O — — — | VDD_IO | ALT2: Reset configuration LPC Port Size 1 | D5 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|---|-------------------------|-------------------|--------------|--|-----|
| EMB_AD05 | 0x27 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD05/NFC_AD05 — RST_CONF_COREPLL6 — | LPC — — | I/O — — | VDD_IO | ALT2: Reset configuration Core PLL Multiplication Factor 0 | B2 |
| EMB_AD06 | 0x26 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD06/NFC_AD06 — RST_CONF_COREPLL5 — | LPC — — | I/O — — | VDD_IO | ALT2: Reset configuration Core PLL Multiplication Factor 1 | C4 |
| EMB_AD07 | 0x25 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD07/NFC_AD07 — RST_CONF_COREPLL4 — | LPC — — | I/O — — | VDD_IO | ALT2: Reset configuration Core PLL Multiplication Factor 2 | C3 |
| EMB_AD08 | 0x24 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD08/NFC_AD08 PSC3_2 RST_CONF_SPMF0 GPIO28 | LPC PSC3 GPIO1 | I/O I/O I/O | VDD_IO | ALT2: Reset configuration System PLL Multiplication Factor 0 | E4 |
| EMB_AD09 | 0x23 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD09/NFC_AD09 PSC3_1 RST_CONF_SPMF1 GPIO27 | LPC PSC3 GPIO1 | I/O I/O I/O | VDD_IO | ALT2: Reset configuration System PLL Multiplication Factor 1 | C2 |
| EMB_AD10 | 0x22 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD10/NFC_AD10 PSC3_0 RST_CONF_SPMF2 GPIO26 | LPC PSC3 GPIO1 | I/O I/O I/O | VDD_IO | ALT2: Reset configuration System PLL Multiplication Factor 2 | D2 |
| EMB_AD11 | 0x21 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD11/NFC_AD11 PSC2_4 RST_CONF_SPMF3 GPIO25 | LPC PSC2 GPIO1 | I/O I/O I/O | VDD_IO | ALT2: Reset configuration | C1 |
| EMB_AD12 | 0x20 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD12/NFC_AD12 PSC2_3 RST_CONF_PREDIV0 GPIO24 | LPC PSC2 GPIO1 | I/O I/O I/O | VDD_IO | ALT2: Reset configuration | E3 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|---------------------------------------|-------------------------|---------------|--------------|---------------------------|-----|
| EMB_AD13 | 0x1F | ALT0 | LPC_AD13/NFC_AD13 | LPC | I/O | VDD_IO | ALT2: Reset configuration | E2 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC2_2 RST_CONF_PREDIV1 GPIO23 | PSC2 GPIO1 | I/O I/O | | | |
| EMB_AD14 | 0x1E | ALT0 | LPC_AD14/NFC_AD14 | LPC | I/O | VDD_IO | ALT2: Reset configuration | H4 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC2_1 RST_CONF_PREDIV2 GPIO22 | PSC2 GPIO1 | I/O I/O | | | |
| EMB_AD15 | 0x1D | ALT0 | LPC_AD15/NFC_AD15 | LPC | I/O | VDD_IO | ALT2: Reset configuration | E1 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC2_0 RST_CONF_SYSOSCEN GPIO21 | PSC2 GPIO1 | I/O I/O | | | |
| EMB_AD16 | 0x1C | ALT0 | LPC_AD16/LPC_A01/NFC | LPC | I/O | VDD_IO | — | F3 |
| | STD_PU | ALT1 ALT2 ALT3 | _WE — — — | — — — | — — — | | | |
| EMB_AD17 | 0x1B | ALT0 | LPC_AD17/LPC_A02/NFC | LPC | I/O | VDD_IO | ALT2: Reset configuration | G3 |
| | STD_PU | ALT1 ALT2 ALT3 | _RE — RST_CONF_PLL_LOCK — | — — — | — — — | | | |
| EMB_AD18 | 0x1A | ALT0 | LPC_AD18/LPC_A03/NFC | LPC | I/O | VDD_IO | ALT2: Reset configuration | G2 |
| | STD_PU | ALT1 ALT2 ALT3 | _CLE — RST_CONF_LPCMX — | — — — | — — — | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|--|-------------------------|-----------------|--------------|---------------------------|-----|
| EMB_AD19 | 0x19 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD19/LPC_A04/NFC_ALE — RST_CONF_LPCWA — | LPC — — | I/O — — | VDD_IO | ALT2: Reset configuration | J4 |
| EMB_AD20 | 0x18 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD20/LPC_A05 — — GPIO20 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | H3 |
| EMB_AD21 | 0x17 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD21/LPC_A06 — — GPIO19 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | F1 |
| EMB_AD22 | 0x16 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD22/LPC_A07 — RST_CONF_LPC_TS GPIO18 | LPC — GPIO1 | I/O — I/O | VDD_IO | ALT2: Reset configuration | K4 |
| EMB_AD23 | 0x15 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD23/LPC_A08 — — GPIO17 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | J3 |
| EMB_AD24 | 0x14 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD24/LPC_A09 — — GPIO16 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | K3 |
| EMB_AD25 | 0x13 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD25/LPC_A10 — — GPIO15 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | G1 |
| EMB_AD26 | 0x12 STD_PU | ALT0 ALT1 ALT2 ALT3 | LPC_AD26/LPC_A11 — — GPIO14 | LPC — GPIO1 | I/O — I/O | VDD_IO | — | J2 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|----------------------------|-------------------------|---------------|--------------|-------|-----|
| EMB_AD27 | 0x11 | ALT0 | LPC_AD27/LPC_A12 | LPC | I/O | VDD_IO | — | M4 |
| | STD_PU | ALT1 ALT2 ALT3 | — — GPIO13 | — — GPIO1 | — — I/O | | | |
| EMB_AD28 | 0x10 | ALT0 | LPC_AD28/LPC_A13 | LPC | I/O | VDD_IO | — | H1 |
| | STD_PU | ALT1 ALT2 ALT3 | — — GPIO12 | — — GPIO1 | — — I/O | | | |
| EMB_AD29 | 0x0F | ALT0 | LPC_AD29/LPC_A14 | LPC | I/O | VDD_IO | — | L3 |
| | STD_PU | ALT1 ALT2 ALT3 | — — GPIO11 | — — GPIO1 | — — I/O | | | |
| EMB_AD30 | 0x0E | ALT0 | LPC_AD30/LPC_A15 | LPC | I/O | VDD_IO | — | M3 |
| | STD_PU_ST | ALT1 ALT2 ALT3 | CAN_CLK — GPIO10 | — — GPIO1 | O — I/O | | | |
| EMB_AD31 | 0x0D | ALT0 | LPC_AD31/LPC_A16 | LPC | I/O | VDD_IO | — | J1 |
| | STD_PU_ST | ALT1 ALT2 ALT3 | PSC_MCLK_IN — GPIO09 | — — GPIO1 | I — I/O | | | |
| EMB_AX00 | 0x0C | ALT0 | LPC_AX00/LPC_ALE | LPC | O | VDD_IO | — | K1 |
| | STD_PU | ALT1 ALT2 ALT3 | — — — | — — — | — — — | | | |
| EMB_AX01 | 0x0B | ALT0 | LPC_AX01/LPC_TSIZE0 | LPC | O | VDD_IO | — | N4 |
| | STD_PU | ALT1 ALT2 ALT3 | — LPC_CS4 — | — LPC — | — O — | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-----------|---|---------------------------------|----------------------------------|-------------------------|-------------------|--------------|--|-----|
| EMB_AX02 | 0x0A | ALT0 | LPC_AX02/LPC_TSIZ1 | LPC | O | VDD_IO | — | L2 |
| | STD_PU | ALT1 ALT2 ALT3 | NFC_CE3 LPC_CS3 — | LPC — | O O — | | | |
| NFC_CE0_B | 0x02D | ALT0 | NFC_CE0 | NFC | O | VDD_IO | — | P1 |
| | STD_PU | ALT1 ALT2 ALT3 | — — GPIO29 | — — GPIO1 | — — I/O | | | |
| NFC_RB | 0x02E | ALT0 | NFC_R/B0 | NFC | I | VDD_IO | When booting from the NFC, the NFC_RB pin needs an external pullup resistor. | N1 |
| | STD_PU_ST | ALT1 ALT2 ALT3 | — — GPIO30 | — — GPIO1 | — — I/O | | | |
| DIU_CLK | 0x02F | ALT0 | DIU_CLK | DIU | O | VDD_IO | — | AB8 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC4_0 USB1_DATA0 LPC_AX04 | PSC4 USB1 LPC | I/O I/O O | | | |
| DIU_DE | 0x030 | ALT0 | DIU_DE | DIU | O | VDD_IO | — | AA8 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC4_1 USB1_DATA1 LPC_AX05 | PSC4 USB1 LPC | I/O I/O O | | | |
| DIU_HSYNC | 0x031 | ALT0 | DIU_HSYNC | DIU | O | VDD_IO | — | W11 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC4_2 USB1_DATA2 LPC_AX06 | PSC4 USB1 LPC | I/O I/O O | | | |
| DIU_VSYNC | 0x032 | ALT0 | DIU_VSYNC | DIU | I/O | VDD_IO | — | Y17 |
| | STD_PU | ALT1 ALT2 ALT3 | PSC4_3 USB1_DATA3 GPIO31 | PSC4 USB1 GPIO1 | I/O I/O I/O | | | |
| DIU_LD00 | 0x033 | ALT0 | CAN3_RX | CAN3 | I | VDD_IO | — | AB9 |
| | STD_PU_ST | ALT1 ALT2 ALT3 | CLK_OUT2 DIU_LD00 GPIO32 | DIU DIU GPIO2 | O I/O I/O | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|--|------------------------------|--------------------------|--------------|-------|------|
| DIU_LD01 | 0x034 STD_PU | ALT0 ALT1 ALT2 ALT3 | CAN3_TX CLK_OUT3 DIU_LD01 GPIO33 | CAN3 DIU DIU GPIO2 | O O I/O I/O | VDD_IO | — | Y10 |
| DIU_LD02 | 0x035 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD02 PSC4_4 USB1_DATA4 LPC_AX07 | DIU PSC4 USB1 LPC | I/O I/O O | VDD_IO | — | AA10 |
| DIU_LD03 | 0x036 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD03 PSC5_0 USB1_DATA5 LPC_AX08 | DIU PSC5 USB1 LPC | I/O I/O I/O O | VDD_IO | — | Y11 |
| DIU_LD04 | 0x037 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD04 PSC5_1 USB1_DATA6 LPC_AX09 | DIU PSC5 USB1 LPC | I/O I/O I/O O | VDD_IO | — | AA11 |
| DIU_LD05 | 0x038 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD05 PSC5_2 USB1_DATA7 GPIO34 | DIU PSC5 USB1 GPIO2 | I/O I/O I/O I/O | VDD_IO | — | AB10 |
| DIU_LD06 | 0x039 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD06 PSC5_3 USB1_STOP GPIO35 | DIU PSC5 USB1 GPIO2 | I/O I/O O I/O | VDD_IO | — | AB11 |
| DIU_LD07 | 0x03A STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | DIU_LD07 PSC5_4 USB1_CLK GPIO36 | DIU PSC5 USB1 GPIO2 | I/O I/O I I/O | VDD_IO | — | Y12 |
| DIU_LD08 | 0x03B STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | CAN4_RX PSC6_0 DIU_LD08 GPIO37 | CAN4 PSC6 DIU GPIO2 | I I/O I/O I/O | VDD_IO | — | W13 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|---|--|--------------------------|--------------|-------|------|
| DIU_LD09 | 0x03C STD_PU | ALT0 ALT1 ALT2 ALT3 | CAN4_TX PSC6_1 DIU_LD09 GPIO38 | CAN4 PSC6 DIU GPIO2 | O I/O I/O I/O | VDD_IO | — | AB12 |
| DIU_LD10 | 0x03D STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD10 PSC6_2 USB1_NEXT GPIO39 | DIU PSC6 USB1 GPIO2 | I/O I/O O I/O | VDD_IO | — | Y13 |
| DIU_LD11 | 0x03E STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD11 PSC6_3 USB1_DIR GPIO40 | DIU PSC6 USB1 GPIO2 | I/O I/O I I/O | VDD_IO | — | AA13 |
| DIU_LD12 | 0x03F STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD12 PSC6_4 USB2_DATA0 GPT2[0] | DIU PSC6 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | AB13 |
| DIU_LD13 | 0x040 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD13 PSC7_0 USB2_DATA1 GPT2[1] | DIU PSC7 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | W14 |
| DIU_LD14 | 0x041 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD14 PSC7_1 USB2_DATA2 GPT2[2] | DIU PSC7 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | Y14 |
| DIU_LD15 | 0x042 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD15 PSC7_2 USB2_DATA3 GPT2[3] | DIU PSC7 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | AB14 |
| DIU_LD16 | 0x043 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | CLK_OUT0 I2C3_SCL DIU_LD16 GPIO41 | DIU I ² C2 DIU GPIO2 | O I/O I/O I/O | VDD_IO | — | AA15 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|----------|---|---------------------------------|---|--|--------------------------|--------------|-------|------|
| DIU_LD17 | 0x044 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | CLK_OUT1 I2C3_SDA DIU_LD17 GPIO42 | DIU I ² C3 DIU GPIO2 | O I/O I/O I/O | VDD_IO | — | Y15 |
| DIU_LD18 | 0x045 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD18 PSC7_3 USB2_DATA4 GPT2[4] | DIU PSC7 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | AB15 |
| DIU_LD19 | 0x046 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD19 PSC7_4 USB2_DATA5 GPT2[5] | DIU PSC7 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | AB16 |
| DIU_LD20 | 0x047 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD20 PSC8_0 USB2_DATA6 GPT2[6] | DIU PSC8 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | AB17 |
| DIU_LD21 | 0x048 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD21 PSC8_1 USB2_DATA7 GPT2[7] | DIU PSC8 USB2 GPT2 | I/O I/O I/O I/O | VDD_IO | — | W16 |
| DIU_LD22 | 0x049 STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD22 PSC8_2 USB2_DIR GPIO43 | DIU PSC8 USB2 GPIO2 | I/O I/O I I/O | VDD_IO | — | Y16 |
| DIU_LD23 | 0x04A STD_PU | ALT0 ALT1 ALT2 ALT3 | DIU_LD23 PSC8_3 USB2_NEXT GPIO44 | DIU PSC8 USB2 GPIO2 | I/O I/O I I/O | VDD_IO | — | AA17 |
| I2C2_SCL | 0x4B STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | I2C2_SCL PSC8_4 USB2_CLK GPIO45 | I ² C2 PSC8 USB2 GPIO2 | I/O I/O I I/O | VDD_IO | — | V4 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------------|---|---------------------------------|--|--|------------------------|--------------|--|-----|
| I2C2_SDA | 0x4C STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | I2C2_SDA PSC9_4 USB2_STOP GPIO46 | I ² C2 PSC9 USB2 GPIO2 | I/O I/O O I/O | VDD_IO | — | U4 |
| I2C1_SCL | 0x4F STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | I2C1_SCL PSC9_2 CAN3_RX GPIO49 | I ² C1 PSC9 CAN3 GPIO2 | I/O I/O I I/O | VDD_IO | — | B18 |
| I2C1_SDA | 0x50 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | I2C1_SDA PSC9_3 CAN3_TX GPIO50 | I ² C1 PSC9 CAN3 GPIO2 | I/O I/O O I/O | VDD_IO | — | A19 |
| CAN1_RX | — | ALT0 ALT1 ALT2 ALT3 | CAN1_RX — — — | CAN1 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | C9 |
| CAN2_RX | — | ALT0 ALT1 ALT2 ALT3 | CAN2_RX — — — | CAN2 — — — | I — — — | VBAT | Dedicated input can be used to receive an external wakeup. | B8 |
| CAN1_TX | 0x4D STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | CAN1_TX PSC9_0 I2C2_SCL GPIO47 | CAN1 PSC9 I ² C2 GPIO2 | O I/O I/O I/O | VDD_IO | — | B15 |
| CAN2_TX | 0x4E STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | CAN2_TX PSC9_1 I2C2_SDA GPIO48 | CAN2 PSC9 I ² C2 GPIO2 | O I/O I/O I/O | VDD_IO | — | A16 |
| FEC1_TXD_2 | 0x51 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_TXD_2 PSC2_0 USB2_DATA0 GPIO51 | FEC1 PSC2 USB2 GPIO2 | O I/O I/O I/O | VDD_IO | — | AA1 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------------|---|---------------------------------|---|-------------------------------|------------------------|--------------|-------|-----|
| FEC1_TXD_3 | 0x52 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_TXD_3 PSC2_1 USB2_DATA1 GPIO52 | FEC1 PSC2 USB2 GPIO2 | O I/O I/O I/O | VDD_IO | — | Y1 |
| FEC1_RXD_2 | 0x53 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_RXD_2 PSC2_2 USB2_DATA2 GPIO53 | FEC1 PSC2 USB2 GPIO2 | I I/O I/O I/O | VDD_IO | — | Y4 |
| FEC1_RXD_3 | 0x54 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_RXD_3 PSC2_3 USB2_DATA3 GPIO54 | FEC1 PSC2 USB2 GPIO2 | I I/O I/O I/O | VDD_IO | — | AA2 |
| FEC1_CR_S | 0x55 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_CR_S PSC2_4 USB2_DATA4 GPIO55 | FEC1 PSC2 USB2 GPIO2 | I I/O I/O I/O | VDD_IO | — | U1 |
| FEC1_TX_ER | 0x56 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_TX_ER PSC3_0 USB2_DATA5 GPIO56 | FEC1 PSC3 USB2 GPIO2 | O I/O I/O I/O | VDD_IO | — | W2 |
| FEC1_RXD_1 | 0x57 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_RXD_1/RMII_RX1 PSC3_1 USB2_DATA6 GPIO57 | FEC1 PSC3 USB2 GPIO2 | I I/O I/O I/O | VDD_IO | — | AA3 |
| FEC1_TXD_1 | 0x58 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_TXD_1/RMII_TX1 PSC3_2 USB2_DATA7 GPIO58 | FEC1 PSC3 USB2 GPIO2 | O I/O I/O I/O | VDD_IO | — | W3 |
| FEC1_MDC | 0x59 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_MDC/RMII_MDC PSC3_3 USB2_DIR GPIO59 | FEC1 PSC3 USB2 GPIO2 | O I/O I I/O | VDD_IO | — | V1 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------------|---|---------------------------------|--|-------------------------------|----------------------|--------------|-------|-----|
| FEC1_RX_ER | 0x5A STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_RX_ER/RMII_RX_ER PSC3_4 USB2_NEXT GPIO60 | FEC1 PSC3 USB2 GPIO2 | I I/O I I/O | VDD_IO | — | Y5 |
| FEC1_MDIO | 0x5B STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_MDIO/RMII_MDIO — USB2_CLK GPIO61 | FEC1 — USB2 GPIO2 | I/O — I I/O | VDD_IO | — | V2 |
| FEC1_RXD_0 | 0x5C STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_RXD_0/RMII_RX0 — USB2_STOP GPIO62 | FEC1 — USB2 GPIO2 | I — O I/O | VDD_IO | — | AB2 |
| FEC1_TXD_0 | 0x5D STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_TXD_0/RMII_TX0 — NFC_R/B1 GPIO63 | FEC1 — NFC GPIO2 | O — I I/O | VDD_IO | — | W4 |
| FEC1_TX_CLK | 0x5E STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_TX_CLK/RMII_REF_CLK PSC0_0 — GPIO04 | FEC1 PSC0 — GPIO1 | I I/O — I/O | VDD_IO | — | W1 |
| FEC1_RX_CLK | 0x5F STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_RX_CLK PSC0_1 NFC_R/B2 GPIO05 | FEC1 PSC0 — GPIO1 | I I/O I I/O | VDD_IO | — | AB4 |
| FEC1_RX_DV | 0x60 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_RX_DV/RMII_CRS_DV PSC0_2 NFC_R/B3 GPIO06 | FEC1 PSC0 NFC GPIO1 | I I/O I I/O | VDD_IO | — | AB3 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------------|---|---------------------------------|--|----------------------------|------------------------|--------------|-------|-----|
| FEC1_TX_EN | 0x61 STD_PU | ALT0 ALT1 ALT2 ALT3 | FEC1_TX_EN/RMII_TX_EN PSC0_3 — GPIO07 | FEC1 PSC0 — GPIO1 | O I/O — I/O | VDD_IO | — | Y3 |
| FEC1_COL | 0x62 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | FEC1_COL PSC0_4 — GPIO08 | FEC1 PSC0 — GPIO1 | I I/O — I/O | VDD_IO | — | U3 |
| USB1_DATA0 | 0x63 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA0 PSC1_0 FEC2_RXD_1/RMII_RX1 — | USB2 PSC1 FEC2 | I/O I/O I — | VDD_IO | — | Y9 |
| USB1_DATA1 | 0x64 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA1 PSC1_1 FEC2_TXD_1/RMII_TX1 — | USB2 PSC1 FEC2 | I/O I/O O — | VDD_IO | — | W9 |
| USB1_DATA2 | 0x65 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA2 PSC1_2 FEC2_MDC/RMII_MDC — | USB2 PSC1 FEC2 | I/O I/O O — | VDD_IO | — | AB7 |
| USB1_DATA3 | 0x66 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA3 PSC1_3 FEC2_RX_ER/RMII_RX_ER — | USB2 PSC1 FEC2 | I/O I/O I — | VDD_IO | — | AB6 |
| USB1_DATA4 | 0x67 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA4 PSC1_4 FEC2_MDIO/RMII_MDIO — | USB2 PSC1 FEC2 | I/O I/O I/O — | VDD_IO | — | AA7 |
| USB1_DATA5 | 0x68 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA5 PSC4_0 FEC2_RXD_0/RMII_RX0 — | USB2 PSC4 FEC2 | I/O I/O I — | VDD_IO | — | Y7 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|------------|---|---------------------------------|---|-------------------------------|----------------------|--------------|-------|-----|
| USB1_DATA6 | 0x69 STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_DATA6 PSC4_1 FEC2_TXD_0/RMII_TX0 — | USB2 PSC4 FEC2 | I/O I/O O — | VDD_IO | — | Y6 |
| USB1_DATA7 | 0x6A STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | USB1_DATA7 PSC4_2 FEC2_TX_CLK/RMII_REF_CLK — | USB2 PSC4 FEC2 | I/O I/O I — | VDD_IO | — | AB5 |
| USB1_STOP | 0x6B STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | USB1_STOP PSC4_3 FEC2_RX_CLK — | USB2 PSC4 FEC2 | O I/O I — | VDD_IO | — | W6 |
| USB1_CLK | 0x6C STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | USB1_CLK PSC4_4 FEC2_RX_DV/RMII_CRSDV — | USB2 PSC4 FEC2 | I I/O I — | VDD_IO | — | Y8 |
| USB1_NEXT | 0x6D STD_PU | ALT0 ALT1 ALT2 ALT3 | USB1_NEXT — FEC2_TX_EN/RMII_TX_EN GPIO09 | USB2 — FEC2 GPIO1 | I — O I/O | VDD_IO | — | AA5 |
| USB1_DIR | 0x6E STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | USB1_DIR — FEC2_COL GPIO10 | USB2 — FEC2 GPIO1 | I — I I/O | VDD_IO | — | W7 |
| SDHC | | | | | | | | |
| SDHC1_CLK | 0x6F STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_CLK NFC_CE1 FEC2_TXD_2 GPIO11 | SDHC1 NFC FEC2 GPIO1 | O O O I/O | VDD_IO | — | T1 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-------------|---|---------------------------------|---|--------------------------------|--------------------------|--------------|-------|-----|
| SDHC1_CMD | 0x70 STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_CMD PSC5_0 FEC2_TXD_3 GPIO12 | SDHC1 PSC5 FEC2 GPIO1 | I/O I/O O I/O | VDD_IO | — | T2 |
| SDHC1_D0 | 0x71 STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_D0 PSC5_1 FEC2_RXD_2 GPIO13 | SDHC1 PSC5 FEC2 GPIO1 | I/O I/O I I/O | VDD_IO | — | T3 |
| SDHC1_D1 | 0x72 STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_D1_IRQ PSC5_2 FEC2_RXD_3 LPC_CS5 | SDHC1 PSC5 FEC2 LPC | I/O I/O I O | VDD_IO | — | T4 |
| SDHC1_D2 | 0x73 STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_D2 PSC5_3 FEC2_CRS LPC_CS6 | SDHC1 PSC5 FEC2 LPC | I/O I/O I O | VDD_IO | — | R1 |
| SDHC1_D3 | 0x74 STD_PU | ALT0 ALT1 ALT2 ALT3 | SDHC1_D3_CD PSC5_4 FEC2_TX_ER LPC_CS7 | SDHC1 PSC5 FEC2 LPC | I/O I/O O O | VDD_IO | — | R2 |
| PSC_MCLK_IN | 0x75 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | PSC_MCLK_IN — — GPIO14 | — — — GPIO1 | I — — I/O | VDD_IO | — | D6 |
| PSC0_0 | 0x76 STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC0_0 SDHC2_CMD GPT1[0] GPIO15 | PSC0 SDHC2 GPT1 GPIO1 | I/O I/O I/O I/O | VDD_IO | — | C11 |
| PSC0_1 | 0x77 STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC0_1 SDHC2_D0 GPT1[1] GPIO16 | PSC0 SDHC2 GPT1 GPIO1 | I/O I/O I/O I/O | VDD_IO | — | A12 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|--------|---|---------------------------------|---|--------------------------------|--------------------------|--------------|-------|-----|
| PSC0_2 | 0x78 STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC0_2 SDHC2_D1_IRQ GPT1[2] GPIO17 | PSC0 SDHC2 GPT1 GPIO1 | I/O I/O I/O I/O | VDD_IO | — | A13 |
| PSC0_3 | 0x79 STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC0_3 SDHC2_D2 GPT1[3] GPIO18 | PSC0 SDHC2 GPT1 GPIO1 | I/O I/O I/O I/O | VDD_IO | — | B13 |
| PSC0_4 | 0x7A STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC0_4 SDHC2_D3_CD GPT1[4] CAN1_TX | PSC0 SDHC2 GPT1 CAN1 | I/O I/O I/O O | VDD_IO | — | D11 |
| PSC1_0 | 0x7B STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC1_0 SDHC2_CLK GPT1[5] CAN2_TX | PSC1 SDHC2 GPT1 CAN2 | I/O O O O | VDD_IO | — | C12 |
| PSC1_1 | 0x7C STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC1_1 CAN_CLK GPT1[6] IRQ0 | PSC1 GPT1 | I/O I/O I | VDD_IO | — | C13 |
| PSC1_2 | 0x7D STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC1_2 TPA2 GPT1[7] IRQ1 | PSC1 GPT1 | I/O I/O I | VDD_IO | — | B14 |
| PSC1_3 | 0x7E STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC1_3 CKSTP_IN NFC_R/B2 GPIO19 | PSC1 NFC GPIO1 | I/O I I/O | VDD_IO | — | D13 |
| PSC1_4 | 0x7F STD_PU | ALT0 ALT1 ALT2 ALT3 | PSC1_4 CKSTP_OUT NFC_CE2 GPIO20 | PSC1 MFC GPIO1 | I/O O I/O | VDD_IO | — | A15 |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|--------------------------|---|---------------------------------|--|--|--------------------|--------------|--|-----|
| J1850_TX | 0x80 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | J1850_TX — NFC_CE3 I2C1_SCL | J1850 — NFC I ² C1 | O — O I/O | VDD_IO | — | B5 |
| J1850_RX | 0x81 STD_PU_ST | ALT0 ALT1 ALT2 ALT3 | J1850_RX — NFC_R \bar{B} 3 I2C1_SDA | J1850 — NFC I ² C1 | I — I I/O | VDD_IO | — | C6 |
| JTAG | | | | | | | | |
| TCK | — | ALT0 ALT1 ALT2 ALT3 | TCK — — — | JTAG — — — | I — — — | VDD_IO | 5. This pin contains an enabled internal Schmitt trigger. | C16 |
| TDI | — | ALT0 ALT1 ALT2 ALT3 | TDI — — — | JTAG — — — | I — — — | VDD_IO | 3. This JTAG pin has an internal pullup P-FET, and cannot be configured. | C15 |
| TDO | — | ALT0 ALT1 ALT2 ALT3 | TDO — — — | JTAG — — — | O — — — | VDD_IO | — | B16 |
| TMS | — | ALT0 ALT1 ALT2 ALT3 | TMS — — — | JTAG — — — | I — — — | VDD_IO | 3. This JTAG pin has an internal pullup P-FET, and cannot be configured. | D15 |
| $\overline{\text{TRST}}$ | — | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{TRST}}$ — — — | JTAG — — — | I — — — | VDD_IO | 3. This JTAG pin has an internal pullup P-FET, and cannot be configured. | D16 |
| System Control | | | | | | | | |

Table 2. MPC5125 Pin Multiplexing (continued)

| Pin | Pad I/O Control Register ¹ and Offset ² | Alternate Function ³ | Functions ⁴ | Peripheral ⁵ | I/O Direction | Power Domain | Notes | Pin |
|-----------------------------|---|---------------------------------|--|-------------------------|------------------|--------------|--|-----|
| $\overline{\text{HRESET}}$ | — | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{HRESET}}$ — — — | — — — | I — — — | VDD_IO | 1. This pin is an input or open-drain output, and have internal pull-up P-FETs. This pin can not be configured. 5. This pin contains an enabled internal schmitt-trigger. | A17 |
| $\overline{\text{PORESET}}$ | — | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{PORESET}}$ — — — | — — — | I — — — | VDD_IO | 1. This pin is an input or open-drain output, and have internal pull-up P-FETs. This pin can not be configured. 2. This pin is an input only. This pin cannot be configured. 5. This pin contains an enabled internal schmitt-trigger. | C17 |
| $\overline{\text{SRESET}}$ | — | ALT0 ALT1 ALT2 ALT3 | $\overline{\text{SRESET}}$ — — — | — — — | I — — — | VDD_IO | 1. This pin is an input or open-drain output, and have internal pull-up P-FETs. This pin can not be configured. 5. This pin contains an enabled internal schmitt-trigger. | A18 |
| Test/Debug | | | | | | | | |
| TEST | — | ALT0 ALT1 ALT2 ALT3 | TEST — — — | — — — | I — — — | VDD_IO | 2. This pin is an input only. This pin cannot be configured. 4. This test pin must be tied to VSS. | D14 |

NOTES:

- ¹ Pins controlled by the STD_PU_ST register have a Schmitt trigger input; pins controlled by the STD_PU register do not. Pins controlled by the IO_CONTROL_MEM register access their alternate function ALT3 by setting the IO_CONTROL_MEM[16BIT] bit. This setting applies to all pins controlled by IO_CONTROL_MEM. Pins not controlled by these registers are indicated with a “—”.
- ² Offset from IOCONTROL_BASE (default is 0xFF40_A000).
- ³ Except where noted in the Notes column, ALT0 is the primary (default) function for each pin after reset.
- ⁴ Alternate functions are chosen by setting the values of the STD_PU[FUNCMUX] bitfields inside the I/O Control module.
 - STD_PU[FUNCMUX] = 00 → ALT0 (default)
 - STD_PU[FUNCMUX] = 01 → ALT1
 - STD_PU[FUNCMUX] = 10 → ALT2
 - STD_PU[FUNCMUX] = 11 → ALT3
 For selecting alternate functions, the STD_PU and STD_PU_ST registers function the same. When no function is available on a pin's given ALT n function (value of STD_PU[FUNCMUX]), it is shown as “—”.
- ⁵ Module included on the MCU.

3.2.1 Power and Ground Supply Summary

Table 3. MPC5125 324 TEPBGA Power/Ground

| Pin Name | Function Description | Voltage ¹ | Package Pin Locations |
|--------------------------------|---|----------------------|--|
| V _{DD} | Supply voltage — e300 core and peripheral logic | 1.4 V | J10, J11, J12, J13, K14, L9, L14, M9, M14, N14, P10, P11, P12, P13 |
| V _{DD_IO} | Supply voltage — I/O buffers | 3.3 V | A14, B9, B12, B17, C5, C14, D3, F2, G4, H2, M2, R3, V3, W5, W15, AA4, AA9, AA12, AA14, AA16, AB18 |
| V _{DD_IO_MEM} | Supply voltage — memory | — ² | B19, C21, D17, D19, G19, H21, P19, R21, T19, V19, W19, Y21, AB20 |
| AV _{DD_FUSEWR} | Power | 3.3 V | D4 |
| AV _{DD_CPLL} | Analog power | 3.3 V | D10 |
| AV _{DD_SPLL} | Analog power | 3.3 V | A11 |
| AV _{DD_OSC_TMPS} | Analog power | 3.3 V | C10 |
| V _{BAT} | Power | 3.3 V | D8 |
| AV _{SS_CPLL} | Analog ground | 0 V | B11 |
| AV _{SS_OSC_TMPS_SPLL} | Analog ground—Double-bonded AV _{SS_OSC_TMPS} and AV _{SS_SPLL} | 0 V | B10 |
| MV _{REF} | Analog input —Voltage reference for SSTL input pads | — ² | N19 |
| MV _{TT0} | Analog input —SSTL(DDR2) termination (ODT) voltage | — ² | W18 |
| MV _{TT1} | Analog input —SSTL(DDR2) termination (ODT) voltage | — ² | R19 |
| MV _{TT2} | Analog input —SSTL(DDR2) termination (ODT) voltage | — ² | M19 |
| MV _{TT3} | Analog input —SSTL(DDR2) termination (ODT) voltage | — ² | K19 |
| V _{SS} | Ground | 0 V | A1, A2, A22, B1, B7, D7, D12, F4, F21, J9, J14, K2, K[9:13], K21, L4, L[10:13], L19, M[10:13], N[9:13], N21, P2, P4, P9, P14, U2, U21, W8, W10, W12, W17, Y2, AA6, AA18, AB1, AB22 |

NOTES:

¹ Nominal voltages.

² Dependent on external memory type. See [Table 3](#)

NOTE

This table indicates only the pins with a permanently enabled internal pullup, pulldown, or Schmitt trigger. Most digital I/O pins can be configured to enable internal pullup, pulldown, or Schmitt trigger. See the *MPC5125 Reference Manual (MPC5125RM)*, “I/O Control” chapter.

4 Electrical and Thermal Characteristics

4.1 DC Electrical Characteristics

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5125 DC electrical characteristics. [Table 4](#) gives the absolute maximum ratings.

Table 4. Absolute Maximum Ratings¹

| Characteristic | Sym | Min | Max | Unit | SpecID |
|---|----------------------------------|------|-------------------------|------|--------|
| Supply voltage — e300 core and peripheral logic | V_{DD} | -0.3 | 1.47 | V | D1.1 |
| Supply voltage — I/O buffers | V_{DD_IO} , $V_{DD_IO_MEM}$ | -0.3 | 3.6 | V | D1.2 |
| Input reference voltage (DDR/DDR2) | MV_{REF} | -0.3 | 3.6 | V | D1.15 |
| Termination Voltage (DDR2) | MV_{TT} | -0.3 | 3.6 | V | D1.16 |
| Supply voltage — system APLL | AV_{DD_SPLL} | -0.3 | 3.6 | V | D1.3 |
| Supply voltage — system oscillator and temperature sensor | $AV_{DD_OSC_TMPS}$ | -0.3 | 3.6 | V | D1.4 |
| Supply voltage — e300 APLL | AV_{DD_CPLL} | -0.3 | 3.6 | V | D1.5 |
| Supply voltage — RTC (hibernation) | V_{BAT} | -0.3 | 3.6 | V | D1.6 |
| Supply voltage — FUSE programming | AV_{DD_FUSEWR} | -0.3 | 3.6 | V | D1.7 |
| Input voltage (V_{DD_IO}) | V_{in} | -0.3 | $V_{DD_IO} + 0.3$ | V | D1.9 |
| Input voltage ($V_{DD_IO_MEM}$) | V_{in} | -0.3 | $V_{DD_IO_MEM} + 0.3$ | V | D1.10 |
| Input voltage (V_{BAT}) | V_{in} | -0.3 | $V_{BAT} + 0.3$ | V | D1.11 |
| Input voltage overshoot | V_{inos} | — | 1 | V | D1.12 |
| Input voltage undershoot | V_{inus} | — | 1 | V | D1.13 |
| Storage temperature range | T_{stg} | -55 | 150 | °C | D1.14 |

NOTES:

¹ Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

4.1.2 Recommended Operating Conditions

[Table 5](#) gives the recommended operating conditions.

Table 5. Recommended Operating Conditions

| Characteristic | Sym | Min ¹ | Typ | Max ¹ | Unit | SpecID |
|---|----------|------------------|-----|------------------|------|--------|
| Supply voltage — e300 core and peripheral logic | V_{DD} | 1.33 | 1.4 | 1.47 | V | D2.1 |
| State retention voltage — e300 core and peripheral logic ² | | 1.08 | — | — | V | D2.2 |

Table 5. Recommended Operating Conditions (continued)

| Characteristic | Sym | Min ¹ | Typ | Max ¹ | Unit | SpecID |
|---|---|-------------------------------|-------------------------------|-------------------------------|------|--------|
| Supply voltage — standard I/O buffers | V_{DD_IO} | 3.0 | 3.3 | 3.6 | V | D2.3 |
| Supply voltage — memory I/O buffers (DDR) | $V_{DD_IO_MEM_DDR}$ | 2.3 | 2.5 | 2.7 | V | D2.4 |
| Supply voltage — memory I/O buffers (DDR2, LPDDR, Mobile SDR) | $V_{DD_IO_MEM_DDR2}$ $V_{DD_IO_MEM_LPDDR}$ | 1.7 | 1.8 | 1.9 | V | D2.5 |
| Supply voltage — memory I/O buffers (SDR) | $V_{DD_IO_MEM_SDR}$ | 3.0 | 3.3 | 3.6 | V | D2.19 |
| Input reference voltage (DDR/DDR2) | MV_{REF} | $0.49 \times V_{DD_IO_MEM}$ | $0.50 \times V_{DD_IO_MEM}$ | $0.51 \times V_{DD_IO_MEM}$ | V | D2.6 |
| Termination voltage (DDR2) | MV_{TT} | $MV_{REF} - 0.04$ | MV_{REF} | $MV_{REF} + 0.04$ | V | D2.7 |
| Supply voltage — system APLL | AV_{DD_SPLL} | 3.0 | 3.3 | 3.6 | V | D2.8 |
| Supply voltage — system oscillator and temperature sensor | $AV_{DD_OSC_TMPS}$ | 3.0 | 3.3 | 3.6 | V | D2.9 |
| Supply voltage — e300 APLL | AV_{DD_CPLL} | 3.0 | 3.3 | 3.6 | V | D2.10 |
| Supply voltage — RTC (hibernation) | V_{BAT}^3 | 3.0 | 3.3 | 3.6 | V | D2.11 |
| Supply voltage — FUSE programming | AV_{DD_FUSEWR} | 3.0 | 3.3 | 3.6 | V | D2.12 |
| Input voltage — standard I/O buffers | V_{in} | 0 | — | V_{DD_IO} | V | D2.14 |
| Input voltage — memory I/O buffers (DDR) | V_{in_DDR} | 0 | — | $V_{DD_IO_MEM_DDR}$ | V | D2.15 |
| Input voltage — memory I/O buffers (DDR2) | V_{in_DDR2} | 0 | — | $V_{DD_IO_MEM_DDR2}$ | V | D2.16 |
| Input voltage — memory I/O buffers (SDR) | V_{in_SDR} | 0 | — | $V_{DD_IO_MEM_SDR}$ | V | D2.20 |
| Input voltage — memory I/O buffers (LPDDR) | V_{in_LPDDR} | 0 | — | $V_{DD_IO_MEM_LPDDR}$ | V | D2.18 |
| Ambient operating temperature range | T_A | -40 | — | +85 | °C | D2.17 |

NOTES:

- ¹ These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.
- ² The State Retention voltage can be applied to VDD after the device is placed in deep-sleep mode.
- ³ VBAT should not be supplied by a battery of voltage less than 3.0 V.

4.1.3 DC Electrical Specifications

Table 6 gives the DC electrical characteristics for the MPC5125 at recommended operating conditions.

Table 6. DC Electrical Specifications

| Characteristic | Condition | Sym | Min | Max | Unit | SpecID |
|--------------------|---|----------|--------------------------|-----|------|--------|
| Input high voltage | Input type = TTL V_{DD_IO} | V_{IH} | $0.51 \times V_{DD_IO}$ | — | V | D3.1 |
| Input high voltage | Input type = TTL $V_{DD_IO_MEM_DDR}$ | V_{IH} | $MV_{REF} + 0.15$ | — | V | D3.2 |

Table 6. DC Electrical Specifications (continued)

| Characteristic | Condition | Sym | Min | Max | Unit | SpecID |
|---|--|---------------|--|--|---------|--------|
| Input high voltage | Input type = TTL $V_{DD_IO_MEM_DDR2}$ | V_{IH} | $MV_{REF} + 0.125$ | — | V | D3.3 |
| Input high voltage | Input type = TTL $V_{DD_IO_MEM_LPDDR}$ | V_{IH} | $0.7 \times V_{DD_IO_MEM_LPDDR}$ | — | V | D3.4 |
| Input high voltage | Input type = TTL $V_{DD_IO_MEM_SDR}$ | V_{IH} | $0.7 \times V_{DD_IO_MEM_SDR}$ | — | V | D3.33 |
| Input high voltage | Input type = Schmitt V_{DD_IO} | V_{IH} | $0.65 \times V_{DD_IO}$ | — | V | D3.5 |
| Input high voltage | SYS_XTALI crystal mode ¹ bypass mode ² | CV_{IH} | $V_{xtal} + 0.4$ $(V_{DD_IO} / 2) + 0.4$ | — | V | D3.6 |
| Input high voltage | RTC_XTALI crystal mode ³ bypass mode ⁴ | RV_{IH} | $(V_{BAT} / 5) + 0.5$ $(V_{BAT} / 2) + 0.4$ | — | V | D3.7 |
| Input low voltage | Input type = TTL V_{DD_IO} | V_{IL} | — | $0.42 \times V_{DD_IO}$ | V | D3.8 |
| Input low voltage | Input type = TTL $V_{DD_IO_MEM_DDR}$ | V_{IL} | — | $MV_{REF} - 0.15$ | V | D3.9 |
| Input low voltage | Input type = TTL $V_{DD_IO_MEM_DDR2}$ | V_{IL} | — | $MV_{REF} - 0.125$ | V | D3.10 |
| Input low voltage | Input type = TTL $V_{DD_IO_MEM_LPDDR}$ | V_{IL} | — | $0.3 \times V_{DD_IO_MEM_LPDDR}$ | V | D3.11 |
| Input low voltage | Input type = TTL $V_{DD_IO_MEM_SDR}$ | V_{IL} | — | $0.3 \times V_{DD_IO_MEM_SDR}$ | V | D3.34 |
| Input low voltage | Input type = Schmitt V_{DD_IO} | V_{IL} | — | $0.35 \times V_{DD_IO}$ | V | D3.12 |
| Input low voltage | SYS_XTALI crystal mode bypass mode | CV_{IL} | — | $V_{xtal} - 0.4 \times (V_{DD_IO}/2) - 0.4$ | V | D3.13 |
| Input low voltage | RTC_XTALI crystal mode bypass mode | RV_{IL} | — | $(V_{BAT}/5) - 0.5$ $(V_{BAT}/2) - 0.4$ | V | D3.14 |
| Input leakage current | $V_{in} = 0$ or $V_{DD_IO}/V_{DD_IO_MEM_DDR/2}$ (depending on input type) ⁵ | I_{IN} | -2.5 | 2.5 | μA | D3.15 |
| Input leakage current | SYS_XTAL_IN $V_{in} = 0$ or V_{DD_IO} | I_{IN} | — | 20 | μA | D3.16 |
| Input leakage current | RTC_XTAL_IN $V_{in} = 0$ or V_{DD_IO} | I_{IN} | — | 1.0 | μA | D3.17 |
| Input current, pullup resistor ⁶ | PULLUP V_{DD_IO} $V_{in} = V_{IL}$ | I_{INpu} | 25 | 150 | μA | D3.18 |
| Input current, pulldown resistor ⁸ | PULLDOWN V_{DD_IO} $V_{in} = V_{IH}$ | I_{INpd} | 25 | 150 | μA | D3.19 |
| Output high voltage | IOH is driver dependent ⁷ V_{DD_IO} | V_{OH} | $0.8 \times V_{DD_IO}$ | — | V | D3.20 |
| Output high voltage | IOH is driver dependent ⁷ $V_{DD_IO_MEM_DDR}$ | V_{OHDDR} | 1.94 | — | V | D3.21 |
| Output high voltage | IOH is driver dependent ⁷ $V_{DD_IO_MEM_DDR2}$ | V_{OHDDR2} | $V_{DD_IO_MEM} - 0.28$ | — | V | D3.22 |
| Output high voltage | IOH is driver dependent ⁷ $V_{DD_IO_MEM_LPDDR}$ | $V_{OHLPDDR}$ | $V_{DD_IO_MEM} - 0.28$ | — | V | D3.23 |

Table 6. DC Electrical Specifications (continued)

| Characteristic | Condition | Sym | Min | Max | Unit | SpecID |
|---|--|---------------|------------------------------|------------------------------|----------|--------|
| Output high voltage | IOH is driver dependent ⁷ $V_{DD_IO_MEM_SDR}$ | V_{OHSDR} | $0.8 \times V_{DD_IO_MEM}$ | — | V | D3.35 |
| Output low voltage | IOL is driver dependent ⁷ V_{DD_IO} | V_{OL} | — | $0.2 \times V_{DD_IO}$ | V | D3.24 |
| Output low voltage | IOL is driver dependent ⁷ $V_{DD_IO_MEM_DDR}$ | V_{OLDDR} | — | 0.36 | V | D3.25 |
| Output low voltage | IOL is driver dependent ⁷ $V_{DD_IO_MEM_DDR2}$ | V_{OLDDR2} | — | 0.28 | V | D3.26 |
| Output low voltage | IOL is driver dependent ⁷ $V_{DD_IO_MEM_LPDDR}$ | $V_{OLLPDDR}$ | — | 0.28 | V | D3.27 |
| Output low voltage | IOL is driver dependent ⁷ $V_{DD_IO_MEM_SDR}$ | V_{OLSDR} | — | $0.2 \times V_{DD_IO_MEM}$ | V | D3.36 |
| DC injection current per pin ⁸ | — | I_{CS} | -1.0 | 1.0 | mA | D3.29 |
| Input capacitance (digital pins) | — | C_{in} | — | 7 | pF | D3.30 |
| Input capacitance (analog pins) | — | C_{in} | — | 10 | pF | D3.31 |
| On-die termination (DDR2) | — | R_{ODT} | 120 | 180 | Ω | D3.32 |

NOTES:

- ¹ This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce the output clock.
- ² This parameter is meant for those who do not use quartz crystals or resonators, but instead use a signal generator clock to drive the clock in bypass mode. In this case, for the oscillator's comparator to produce the output clock, drive only the EXTAL pin. Do not connect anything to any other oscillator pin.
- ³ This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode to drive the clock. In that case, for the oscillator's comparator to produce the output clock, drive one of the XTAL_IN or XTAL_OUT pins. Do not connect anything to the other oscillator pins.
- ⁴ This parameter is meant for those who do not use quartz crystals or resonators, but instead use a signal generator clock to drive the clock in bypass mode. In that case, for the oscillator's comparator to produce the output clock, drive only the XTAL_IN pin. Do not connect anything to any other oscillator pin.
- ⁵ Leakage current is measured with output drivers disabled and with pullups and pulldowns inactive.
- ⁶ Pullup current is measured at V_{IL} and pulldown current is measured at V_{IH} .
- ⁷ See [Table 7](#) for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in [Table 2](#).
- ⁸ All injection current is transferred to $V_{DD_IO}/V_{DD_IO_MEM}$. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 7. General I/O Pads¹ — Drive Current, Slew Rate

| Pad Type | Supply Voltage | Drive Select/Slew Rate Control | Rise time max (ns) | Fall time max (ns) | Current loh (mA) | Current lol (mA) | SpecID |
|------------|-----------------------------|--------------------------------|--------------------|--------------------|------------------|------------------|--------|
| General IO | $V_{DD_IO} = 3.3\text{ V}$ | Configuration 3 (11) | 1.4 | 1.6 | 35 | 35 | D3.41 |
| | | Configuration 2 (10) | 9.8 | 12 | | | D3.42 |
| | | Configuration 1 (01) | 19 | 24 | | | D3.43 |
| | | Configuration 0 (00) | 140 | 183 | | | D3.44 |

NOTES:

¹ General I/O—rise and fall times at drive load 50 pF.

Table 8. DDR I/O Pads¹ — Drive Current, Slew Rate

| Pad Type | Supply Voltage | Drive Select/Slew Rate Control | Rising slew max (ns) ² | Falling slew max (ns) ³ | Current loh (mA) | Current lol (mA) | SpecID |
|----------|--|--------------------------------|-----------------------------------|------------------------------------|------------------|------------------|--------|
| DDR | $V_{DD_IO_MEM} = 2.5\text{ V}$ (DDR) | Configuration 3 (011) | 0.45 | 0.45 | 16.2 | 16.2 | D3.45 |
| | $V_{DD_IO_MEM} = 1.8\text{ V}$ (LPDDR and SDR) | Configuration 0 (000) | 0.8 | 0.8 | 4.6 | 4.6 | D3.46 |
| | | Configuration 1 (001) | | | 8.1 | 8.1 | D3.47 |
| | $V_{DD_IO_MEM} = 1.8\text{ V}$ (DDR2) | Configuration 2 (010) | 0.7 | 0.7 | 5.3 | 5.3 | D3.48 |
| | | Configuration 6 (110) | | | 13.4 | 13.4 | D3.49 |
| | $V_{DD_IO_MEM} = 3.3\text{ V}$ (SDR) | Configuration 7 (111) | 0.45 | 0.45 | 8 | 8 | D3.50 |

NOTES:

¹ DDR—rise and fall times at 50 Ω transmission line impedance terminated to $MV_{TT} (0.5 \times V_{DD_IO_MEM}) + 4\text{ pF}$ load.

² Rising slew rate measured between $0.5 \times V_{DD_IO_MEM} - 450\text{ mV}$ and $0.5 \times V_{DD_IO_MEM} + 50\text{ mV}$ for all modes.

³ Falling slew rate measured between $0.5 \times V_{DD_IO_MEM} + 50\text{ mV}$ and $0.5 \times V_{DD_IO_MEM} - 450\text{ mV}$ for all modes.

4.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or V_{DD}). Table 11 gives package thermal characteristics for this device.

Table 9. ESD and Latch-Up Protection Characteristics

| Sym | Rating | Min | Max | Unit | SpecID |
|-----------|---|------|-----|------|--------|
| V_{HBM} | Human body model (HBM) — JEDEC JESD22-A114-B | 2000 | — | V | D4.1 |
| V_{MM} | Machine model (MM) — JEDEC JESD22-A115 | 200 | — | V | D4.2 |
| V_{CDM} | Charge device model (CDM) — JEDEC JESD22-C101 | 250 | — | V | D4.3 |

4.1.5 Power Dissipation

Power dissipation of the MPC5125 is caused by three different components:

- Dissipation of the internal or core digital logic (supplied by V_{DD})
- Dissipation of the analog circuitry (supplied by AV_{DD_SPLL} and AV_{DD_CPLL})
- Dissipation of the IO logic (supplied by $V_{DD_IO_MEM}$ and V_{DD_IO})

Table 10 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins cannot be given in general, but must be calculated for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_M N \times C \times V_{DD_IO}^2 \times f \tag{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, V_{DD_IO} is the IO voltage swing, f is the switching frequency, and P_{IOint} is the power consumed by the unloaded IO stage. The total power consumption of the MPC5125 device must not exceed this value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} \tag{Eqn. 2}$$

Table 10. Power Dissipation

| Core Power Supply (V_{DD_core}) ¹ | | | | |
|--|-------------------------------|-------------------|------|--------|
| Mode | High-Performance | | Unit | SpecID |
| | e300 = 400 MHz, CSB = 200 MHz | | | |
| Operational ² | 620 | | mW | D5.1 |
| Doze ³ | 580 | | mW | D5.3 |
| Nap ³ | 235 | | mW | D5.2 |
| Sleep ³ | 230 | | mW | D5.4 |
| Deep-sleep ⁴ | 38 | | mW | D5.5 |
| RTC Power Supply (V_{BAT}) | | | | |
| Hibernation | 20 | | μW | D5.6 |
| PLL/OSC Power Supplies (AV_{DD_SPLL} , AV_{DD_CPLL} , $AV_{DD_OSC_TMPS}$) ⁵ | | | | |
| Operational | 18 | | mW | D5.7 |
| Deep-sleep | 55 | | μW | D5.8 |
| Unloaded I/O Power Supplies (V_{DD_IO} , $V_{DD_IO_MEM}$) ⁶ | | | | |
| | V_{DD_IO} | $V_{DD_IO_MEM}$ | | |
| Operational | 180 | 40 | mW | D5.9 |
| Deep-sleep | 5 | 1 | mW | D5.10 |

NOTES:

¹ Typical core power is measured at $V_{DD_core} = 1.4\text{ V}$, $T_J = 25\text{ °C}$.

² Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with DDR write operation.

- ³ Doze, Nap, and Sleep power are measured with the e300 core in Doze/Nap/Sleep mode; the system oscillator, system PLL, and core PLL active; and all other system modules inactive.
- ⁴ Deep-sleep power is measured with the e300 core in Sleep mode. The system oscillator, system PLL, core PLL, and other system modules are inactive.
- ⁵ PLL power is measured at $V_{DD_SPLL} = V_{DD_CPLL} = V_{DD_OSC_TMPS} = 3.3\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$.
- ⁶ Unloaded typical I/O power is measured at $V_{DD_IO} = 3.3\text{ V}$, $V_{DD_MEM_IO} = 1.8\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$.

NOTE

The maximum power depends on the supply voltage, process corner, junction temperature, and the concrete application and clock configurations.

4.1.6 Thermal Characteristics

Table 11. Thermal Resistance Data¹

| Rating | Conditions | Sym | Value | Unit | SpecID |
|--|---|------------------|-------|--------------------|--------|
| Thermal resistance junction-to-ambient natural convection ² | Single layer board – 1s | $R_{\theta JA}$ | 35 | $^\circ\text{C/W}$ | D6.1 |
| Thermal resistance junction-to-ambient natural convection ² | Four layer board – 2s2p | $R_{\theta JA}$ | 25 | $^\circ\text{C/W}$ | D6.2 |
| Thermal resistance junction-to-moving-air ambient ² | @ 200 ft./min., single layer board – 1s | $R_{\theta JMA}$ | 29 | $^\circ\text{C/W}$ | D6.3 |
| Thermal resistance junction-to-moving-air ambient ² | @ 200 ft./min., four layer board 2s2p | $R_{\theta JMA}$ | 22 | $^\circ\text{C/W}$ | D6.4 |
| Thermal resistance junction-to-board ³ | — | $R_{\theta JB}$ | 16 | $^\circ\text{C/W}$ | D6.5 |
| Thermal resistance junction-to-case ⁴ | — | $R_{\theta JC}$ | 11 | $^\circ\text{C/W}$ | D6.6 |
| Junction-to-package-top natural convection ⁵ | Natural convection | Ψ_{JT} | 3 | $^\circ\text{C/W}$ | D6.7 |

NOTES:

- ¹ Thermal characteristics are targets based on simulation that are subject to change per device characterization.
- ² Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
- ³ Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
- ⁴ Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- ⁵ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J , can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{Eqn. 3}$$

where:

- T_A = ambient temperature for the package ($^\circ\text{C}$)
- $R_{\theta JA}$ = junction to ambient thermal resistance ($^\circ\text{C/W}$)
- P_D = power dissipation in package (W)

Electrical and Thermal Characteristics

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package ($^{\circ}\text{C}$)

Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.2 Oscillator and PLL Electrical Characteristics

The MPC5125 system requires a system-level clock input SYS_XTALI. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent real-time clock (RTC) system.

The MPC5125 clock generation uses two phase-locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

4.2.1 System Oscillator Electrical Characteristics

Table 12. System Oscillator Electrical Characteristics

| Characteristic | Sym | Min | Typical | Max | Unit | SpecID |
|--------------------|------------------------|------|---------|------|------|--------|
| SYS_XTAL frequency | $f_{\text{sys_xtal}}$ | 15.6 | 33.3 | 35.0 | MHz | O1.1 |

The system oscillator can work in oscillator mode or in bypass mode to support an external input clock as clock reference.

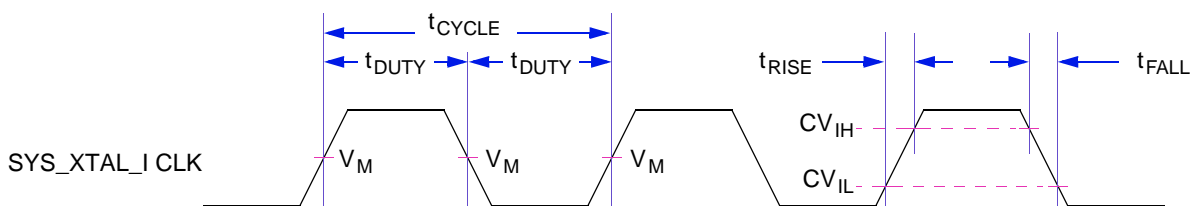


Figure 4. Timing Diagram — SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

| Sym | Description | Min | Max | Units | SpecID |
|--------------------|--|------|-------|-------|--------|
| t_{CYCLE} | SYS_XTALI cycle time ^{1,2} | 64.1 | 28.57 | ns | O.1.2 |
| t_{RISE} | SYS_XTALI rise time ³ | 1 | 4 | ns | O.1.3 |
| t_{FALL} | SYS_XTALI fall time ⁴ | 1 | 4 | ns | O.1.4 |
| t_{DUTY} | SYS_XTALI duty cycle (measured at V_M) ⁵ | 40 | 60 | % | O.1.5 |

NOTES:

- ¹ The SYS_XTALI frequency and system PLL settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the MPC5125 Reference Manual (MPC5125RM).
- ² The min/max cycle times are calculated using $1/f_{\text{sys_xtal}}$ (MIN/MAX) where the $f_{\text{sys_xtal}}$ (MIN/MAX) (15.6 / 35 MHz) are taken from Table 12 (system oscillator electrical characteristics).
- ³ Rise time is measured from 20% of VDD to 80% of VDD.
- ⁴ Fall time is measured from 20% of VDD to 80% of VDD.
- ⁵ SYS_XTALI duty cycle is measured at V_M .

4.2.2 RTC Oscillator Electrical Characteristics

Table 14. RTC Oscillator Electrical Characteristics

| Characteristic | Sym | Min | Typical | Max | Unit | SpecID |
|--------------------|------------------------|-----|---------|-----|------|--------|
| RTC_XTAL frequency | $f_{\text{rtc_xtal}}$ | — | 32.768 | — | kHz | O2.1 |

4.2.3 System PLL Electrical Characteristics

Table 15. System PLL Specifications

| Characteristic | Sym | Min | Typical | Max | Unit | SpecID |
|--|--------------------------|-----|---------|-----|------|--------|
| Sys PLL input clock frequency ¹ | $f_{\text{sys_xtal}}$ | 16 | 33.3 | 67 | MHz | O3.1 |
| Sys PLL input clock jitter ² | t_{jitter} | — | — | 10 | ps | O3.2 |
| Sys PLL VCO frequency ¹ | f_{VCOsys} | 400 | — | 800 | MHz | O3.3 |
| Sys PLL VCO output jitter (Dj), peak to peak / cycle | $f_{\text{VCOjitterDj}}$ | — | — | 40 | ps | O3.4 |
| Sys PLL VCO output jitter (Rj), RMS 1 sigma | $f_{\text{VCOjitterRj}}$ | — | — | 12 | ps | O3.5 |
| Sys PLL relock time — after power up ³ | t_{lock1} | — | — | 200 | μs | O3.6 |
| Sys PLL relock time — when power was on ⁴ | t_{lock2} | — | — | 170 | μs | O3.7 |

NOTES:

- ¹ The SYS_XTAL frequency and PLL configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
- ² This represents total input jitter — short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
- ³ PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
- ⁴ PLL-relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

4.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 16. e300 PLL Specifications

| Characteristic | Sym | Min | Typical | Max | Unit | SpecID |
|-------------------------------------|-----------------------|-----|---------|-----|------|--------|
| e300 frequency ^{1, 2} | f_{core} | 200 | — | 400 | MHz | O4.1 |
| e300 PLL VCO frequency ¹ | f_{VCOcore} | 400 | — | 800 | MHz | O4.3 |
| e300 PLL input clock frequency | $f_{\text{CSB_CLK}}$ | 50 | — | 200 | MHz | O4.4 |
| e300 PLL input clock cycle time | $t_{\text{CSB_CLK}}$ | 5 | — | 20 | ns | O4.5 |
| e300 PLL relock time ³ | t_{lock} | — | — | 200 | μs | O4.6 |

NOTES:

- ¹ The frequency and e300 PLL configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in [Table 17](#).
- ² The following hard-coded relationship exists between f_{core} and f_{VCOcore} : ($f_{\text{core}} = f_{\text{VCOcore}}$).
- ³ PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

4.3 AC Electrical Characteristics

4.3.1 Overview

The following list provides hyperlinks to the indicated timing specification sections.

- AC Operating Frequency Data
- Resets
- SDRAM (DDR)
- LPC
- NFC
- FEC
- USB ULPI
- MMC/SD/SDIO Card Host Controller (SDHC)
- DIU
- CAN
- I²C
- J1850
- PSC
- GPIOs and Timers
- Fusebox
- IEEE 1149.1 (JTAG)

AC test timing conditions:

Unless otherwise noted, all test conditions are as follows:

- $T_A = -40$ to 85 °C
- $V_{DD} = 1.33$ to 1.47 V
 $V_{DD_IO} = 3.0$ to 3.6 V
- Input conditions:
All inputs: $t_{rise}, t_{fall} \leq 1$ ns
- Output Loading:
All outputs: 50 pF

4.3.2 AC Operating Frequency Data

Table 17 provides the operating frequency information for the MPC5125.

Table 17. Clock Frequencies

| | Min | Max | Units | SpecID |
|---------------------|------|-----|-------|--------|
| e300 Processor Core | 200 | 400 | MHz | A1.1 |
| SDRAM clock | 50 | 200 | MHz | A1.2 |
| CSB bus clock | 50 | 200 | MHz | A1.3 |
| IP bus clock | 8.3 | 66 | MHz | A1.4 |
| LPC clock | 2.08 | 66 | MHz | A1.6 |
| NFC clock | 3.13 | 50 | MHz | A1.7 |
| DIU clock | 0.78 | 66 | MHz | A1.8 |
| SDHC clock | 0.78 | 50 | MHz | A1.9 |
| CLKx | 0.78 | 66 | MHz | A1.10 |

NOTES:

Electrical and Thermal Characteristics

1. The SYS_XTAL_IN frequency, Sys PLL, and Core PLL settings must be chosen so that the resulting e300 clk, csb_clk, and MCK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The values are valid for the user-operation mode. There can be deviations for test modes.
3. When selecting the peripheral clock frequencies, care needs to be taken about requirements for baud rates and minimum frequency limitation.
4. The DDR data rate is 2x the DDR memory bus frequency.

SYS_XTAL_IN is the input clock multiplied by the system phase-locked loop (Sys PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the clocks for the peripherals. The csb_clk serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the csb_clk frequency to create the internal clock for the e300 core (core_clk). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word, which is loaded at power-on reset.

See the *MPC5125 Reference Manual (MPC5125RM)*, for more information on the clock subsystem.

4.3.3 Resets

The MPC5125 has three reset pins:

- $\overline{\text{PORESET}}$ — Power-on reset
- $\overline{\text{HRESET}}$ — Hard reset
- $\overline{\text{SRESET}}$ — Software reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5125 inputs, as specified in [Section 4.1, “DC Electrical Characteristics.”](#)

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 18. Reset Rise / Fall Timing

| Description | Min | Max | Unit | SpecID |
|---|-----|-----|------|--------|
| $\overline{\text{PORESET}}$ ¹ fall time | — | 1 | ms | A3.4 |
| $\overline{\text{PORESET}}$ rise time | — | 1 | ms | A3.5 |
| $\overline{\text{HRESET}}$ ^{2,3} fall time | — | 1 | ms | A3.6 |
| $\overline{\text{HRESET}}$ rise time | — | 1 | ms | A3.7 |
| $\overline{\text{SRESET}}$ fall time | — | 1 | ms | A3.8 |
| $\overline{\text{SRESET}}$ rise time | — | 1 | ms | A3.9 |

NOTES:

- ¹ Make sure that the $\overline{\text{PORESET}}$ does not carry any glitches. The MPC5125 has no filter to prevent them from getting into the chip.
- ² $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time.
- ³ The assertion of $\overline{\text{HRESET}}$ becomes active at power-on reset without any SYS_XTAL clock.

The timing relationship can be seen in the following figures.

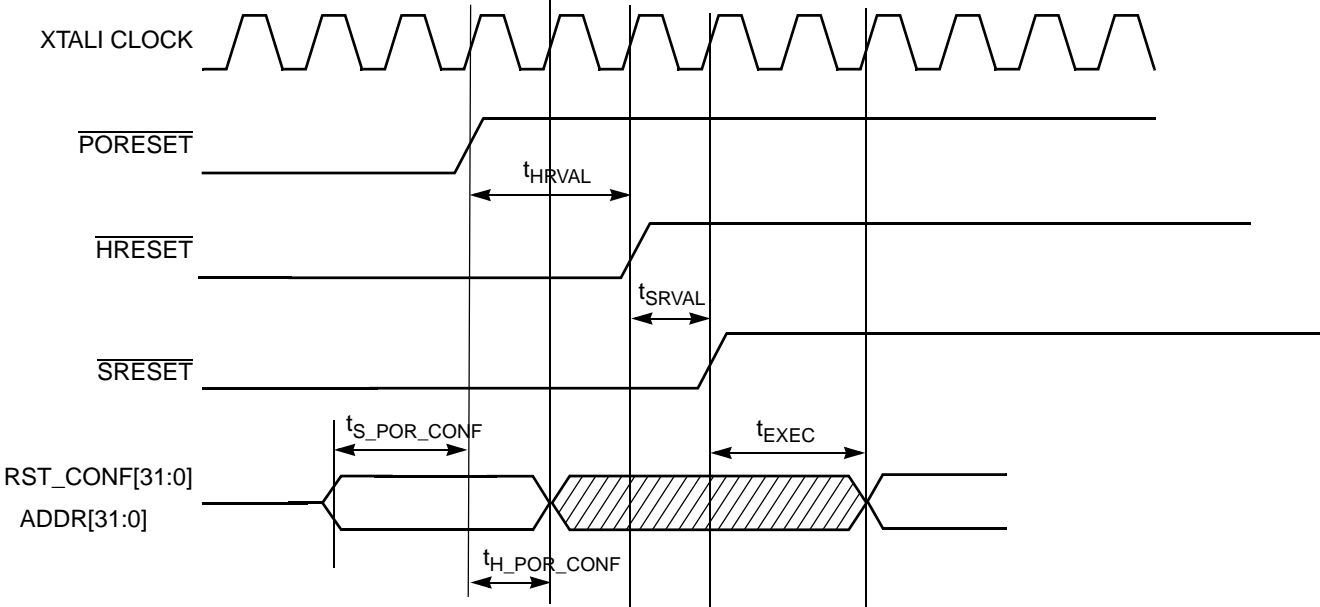


Figure 5. Power-Up Behavior

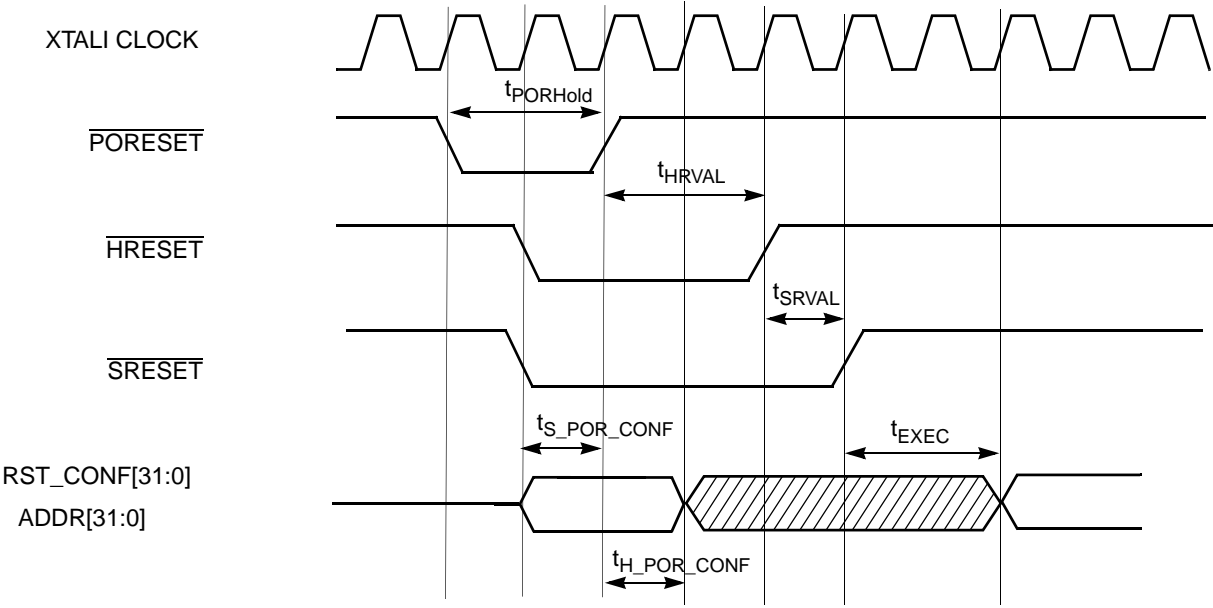


Figure 6. Power-On Reset Behavior

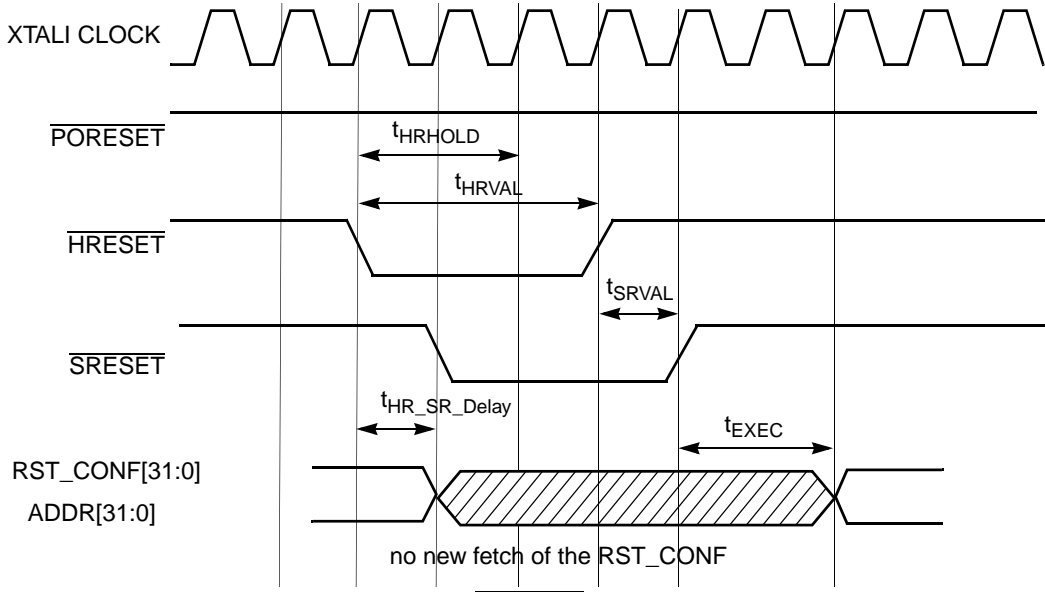


Figure 7. HRESET Behavior

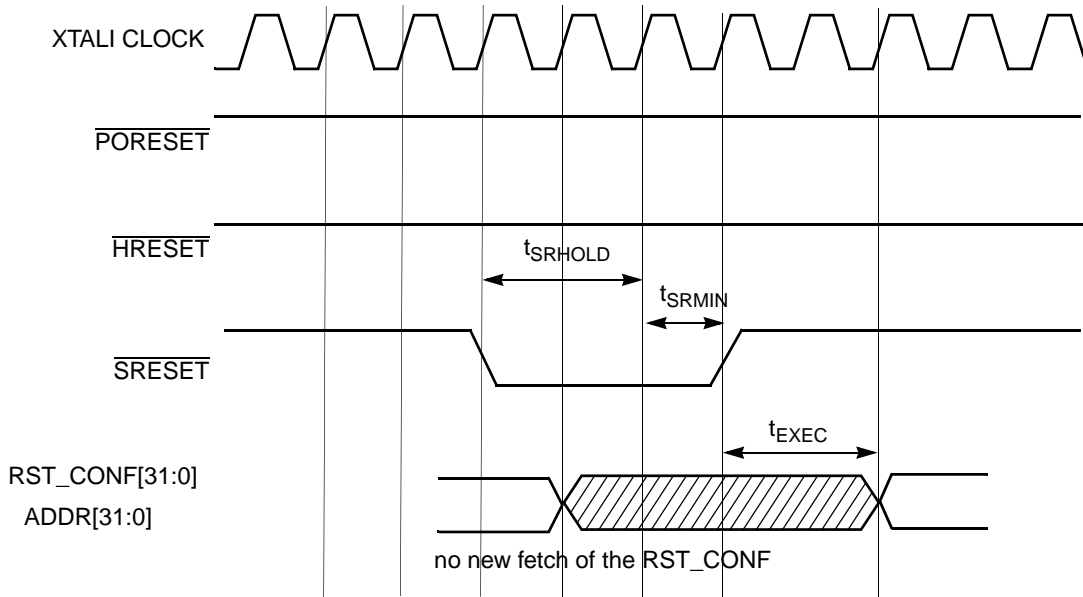


Figure 8. SRESET Behavior

Table 19. Reset Timing

| Symbol | Description | Value (XTALI CLOCK) | SpecID |
|--------------------|---|---------------------------|--------|
| $t_{PORHOLD}$ | Time $\overline{PORESET}$ must be held low before a qualified reset occurs. | 4 cycles | A3.10 |
| t_{HRVAL} | Time \overline{HRESET} is asserted after a qualified reset occurs. | 26810 cycles ¹ | A3.11 |
| t_{SRVAL} | Time \overline{SRESET} is asserted after assertion of \overline{HRESET} . | 21 cycles | A3.12 |
| t_{EXEC} | Time between \overline{SRESET} assertion and first core instruction fetch. | 4 cycles | A3.13 |
| $t_{S_POR_CONF}$ | Reset configuration setup time before assertion of $\overline{PORESET}$. | 1 cycle | A3.14 |

Table 19. Reset Timing (continued)

| Symbol | Description | Value (XTALI CLOCK) | SpecID |
|---------------------|--|---------------------|--------|
| $t_{H_POR_CONF}$ | Reset configuration hold time after assertion of $\overline{PORESET}$. | 1 cycle | A3.15 |
| $t_{HR_SR_DELAY}$ | Time from falling edge of \overline{HRESET} to falling edge of \overline{SRESET} . | 4 cycles | A3.16 |
| t_{HRHOLD} | Time \overline{HRESET} must be held low before a qualified reset occurs. | 4 cycles | A3.17 |
| t_{SRHOLD} | Time \overline{SRESET} must be held low before a qualified reset occurs. | 4 cycles | A3.18 |
| t_{SRMIN} | Time \overline{SRESET} is asserted after it has been qualified. | 1 cycles | A3.19 |

NOTES:

¹ The timings will change when using the PLL lock detection circuit.

4.3.4 External Interrupts

The MPC5125 provides three different kinds of external interrupts:

- IRQ interrupts
- GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Wakeup interrupts

Table 20. IPIC Input AC Timing Specifications

| Descriptions | Symbol | Min | Unit | Spec ID |
|-----------------------------------|--------------|-----|------|---------|
| IPIC inputs — minimum pulse width | t_{PICWID} | 2T | ns | A4.1 |

IPIC inputs must be valid for at least t_{PICWID} to ensure proper operation in edge-triggered mode.

4.3.5 SDRAM (DDR)

The MPC5125 memory controller supports these types of DDR devices:

- DDR-1 (SSTL_2 class II interface)
- DDR-2 (SSTL_18 interface)
- LPDDR (1.8V I/O supply voltage)
- SDR D-RAM

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC standard, DDR2 SDRAM specification, JESD79-2C, May 2006
- JEDEC standard, Double Data Rate (DDR) SDRAM specification, JESD79E, May 2005
- JEDEC standard, Low Power Double Data Rate (LPDDR) SDRAM specification, JESD79-4, May 2006

The MPC5125 supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The MPC5125 memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in [Section 4.1, “DC Electrical Characteristics.”](#)

4.3.5.1 DDR SDRAM AC Timing Specifications

Table 21. DDR SDRAM Timing Specifications
At recommended operating conditions with $V_{DD_IO_MEM}$ of $\pm 5\%$

| Parameter | Symbol | Min | Max | Unit | Notes | SpecID |
|---|-----------------|---------------------------------------|---------------------------------------|----------|-----------|--------|
| Clock cycle time, CL = x | t_{CK} | 6000 | — | ps | | A5.1 |
| MCK AC differential crosspoint voltage | V_{OX-AC} | $(V_{DD_IO_MEM} \times 0.5) - 0.15$ | $(V_{DD_IO_MEM} \times 0.5) + 0.15$ | V | 1 | A5.2 |
| CK HIGH pulse width | t_{CH} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.3 |
| CK LOW pulse width | t_{CL} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.4 |
| Skew between MCK and DQS transitions | t_{DQSS} | -0.25 | 0.25 | t_{CK} | 2,3 | A5.5 |
| Address and control output setup time relative to MCK rising edge | $t_{OS(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.6 |
| Address and control output hold time relative to MCK rising edge | $t_{OH(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.7 |
| DQ and DM output setup time relative to DQS | $t_{DS1(base)}$ | $t_{CK}/4 - 750$ | — | ps | 2,3 | A5.8 |
| DQ and DM output hold time relative to DQS | $t_{DH1(base)}$ | $t_{CK}/4 - 750$ | — | ps | 2,3 | A5.9 |
| DQS-DQ skew for DQS and associated DQ inputs | t_{DQSQ} | $-(t_{CK}/4 - 600)$ | $t_{CK}/4 - 600$ | ps | 3 | A5.10 |
| DQS window position related to CAS read command | t_{DQSEN} | $2t_{CK} + 1500$ | $3t_{CK} - 1000$ | ps | 1,2,3,4,5 | A5.11 |

NOTES:

- ¹ Measured with clock pin loaded with differential 100 Ω termination resistor.
- ² Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD_IO_MEM}/2$.
- ³ All transitions measured at mid-supply ($V_{DD_IO_MEM}/2$).
- ⁴ In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
- ⁵ The window position is given for $t_{DQSEN} = 2.0 t_{CK}$ (RDLY = 2, HALF DQS DLY = QUART DQS DLY = 0) with CL = 3 DDR SDRAM device. For other values of t_{DQSEN} , the window position is shifted accordingly.

4.3.5.2 MobileDDR/LPDDR SDRAM AC Timing Specifications

Table 22. MobileDDR/LPDDR SDRAM Timing Specifications
At recommended operating conditions with $V_{DD_IO_MEM}$ of $\pm 5\%$

| Parameter | Symbol | Min | Max | Unit | Notes | SpecID |
|---|----------------|--------------------------------------|--------------------------------------|----------|-------|--------|
| Clock cycle time, CL = x | t_{CK} | 6000 | — | ps | | A5.1 |
| MCK AC differential crosspoint voltage | V_{OX-AC} | $(V_{DD_IO_MEM} \times 0.5) - 0.1$ | $(V_{DD_IO_MEM} \times 0.5) + 0.1$ | V | 1 | A5.2 |
| CK HIGH pulse width | t_{CH} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.3 |
| CK LOW pulse width | t_{CL} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.4 |
| Skew between MCK and DQS transitions | t_{DQSS} | -0.25 | 0.25 | t_{CK} | 2,3 | A5.5 |
| Address and control output setup time relative to MCK rising edge | $t_{OS(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.6 |

Table 22. MobileDDR/LPDDR SDRAM Timing Specifications (continued)

 At recommended operating conditions with $V_{DD_IO_MEM}$ of $\pm 5\%$

| Parameter | Symbol | Min | Max | Unit | Notes | SpecID |
|--|-----------------|---------------------|------------------|------|-----------|--------|
| Address and control output hold time relative to MCK rising edge | $t_{OH(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.7 |
| DQ and DM output setup time relative to DQS | $t_{DS1(base)}$ | $t_{CK}/4 - 750$ | — | ps | 2,3 | A5.8 |
| DQ and DM output hold time relative to DQS | $t_{DH1(base)}$ | $t_{CK}/4 - 750$ | — | ps | 2,3 | A5.9 |
| DQS-DQ skew for DQS and associated DQ inputs | t_{DQSQ} | $-(t_{CK}/4 - 600)$ | $t_{CK}/4 - 600$ | ps | 3 | A5.10 |
| DQS window position related to CAS read command | t_{DQSEN} | $2t_{CK} - 500$ | $3t_{CK} - 1000$ | ps | 1,2,3,4,5 | A5.11 |

NOTES:

- ¹ Measured with clock pin loaded with differential $100\ \Omega$ termination resistor.
- ² Measured with all outputs except the clock loaded with $50\ \Omega$ termination resistor to $V_{DD_IO_MEM}/2$.
- ³ All transitions measured at mid-supply ($V_{DD_IO_MEM}/2$).
- ⁴ In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
- ⁵ The window position is given for $t_{DQSEN} = 2.0 t_{CK}$ (RDLY = 2, HALF DQS DLY = QUART DQS DLY = 0) with CL = 3 MobileDDR/LPDDR SDRAM device. For other values of t_{DQSEN} , the window position is shifted accordingly.

4.3.5.3 DDR2 SDRAM AC Timing Specifications

Table 23. DDR2 (DDR2-400) SDRAM Timing Specifications

 At recommended operating conditions with $V_{DD_IO_MEM}$ of $\pm 5\%$

| Parameter | Symbol | Min | Max | Unit | Notes | SpecID |
|---|-----------------|--------------------------------------|--------------------------------------|----------|-----------|--------|
| Clock cycle time, CL = x | t_{CK} | 5000 | — | ps | | A5.1 |
| MCK AC differential crosspoint voltage | V_{OX-AC} | $(V_{DD_IO_MEM} \times 0.5) - 0.1$ | $(V_{DD_IO_MEM} \times 0.5) + 0.1$ | V | 1 | A5.2 |
| CK HIGH pulse width | t_{CH} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.3 |
| CK LOW pulse width | t_{CL} | 0.47 | 0.53 | t_{CK} | 1,3 | A5.4 |
| Skew between MCK and DQS transitions | t_{DQSS} | -0.25 | 0.25 | t_{CK} | 2,3 | A5.5 |
| Address and control output setup time relative to MCK rising edge | $t_{OS(base)}$ | $t_{CK}/2 - 750$ | — | ps | 2,3 | A5.6 |
| Address and control output hold time relative to MCK rising edge | $t_{OH(base)}$ | $t_{CK}/2 - 750$ | — | ps | 2,3 | A5.7 |
| DQ and DM output setup time relative to DQS | $t_{DS1(base)}$ | $t_{CK}/4 - 500$ | — | ps | 2,3 | A5.8 |
| DQ and DM output hold time relative to DQS | $t_{DH1(base)}$ | $t_{CK}/4 - 500$ | — | ps | 2,3 | A5.9 |
| DQS-DQ skew for DQS and associated DQ inputs | t_{DQSQ} | $-(t_{CK}/4 - 600)$ | $t_{CK}/4 - 600$ | ps | 3 | A5.10 |
| DQS window position related to CAS read command | t_{DQSEN} | $2.5t_{CK}$ | $3t_{CK} + 1500$ | ps | 1,2,3,4,5 | A5.11 |

Electrical and Thermal Characteristics

NOTES:

- ¹ Measured with clock pin loaded with differential 100 Ω termination resistor.
- ² Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD_IO_MEM}/2$.
- ³ All transitions measured at mid-supply ($V_{DD_IO_MEM}/2$).
- ⁴ In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
- ⁵ The window position is given for $t_{DQSEN} = 2.5 t_{CK}$ (RDLY = 2, HALF DQS DLY = 1, QUART DQS DLY = 0) with CL = 3 DDR2 SDRAM device. For other values of t_{DQSEN} , the window position is shifted accordingly.

4.3.5.4 SDR SDRAM AC Timing Specifications

Table 24. SDR SDRAM Timing Specifications

At recommended operating conditions with $V_{DD_IO_MEM}$ of $\pm 5\%$

| Parameter | Symbol | Min | Max | Unit | Notes | SpecID |
|--|----------------|-------------------|------|----------|--------------|--------|
| Clock cycle time, CL = x | t_{CK} | 7500 | — | ps | | A5.1 |
| CK HIGH pulse width | t_{CH} | 0.43 | 0.57 | t_{CK} | 1,3 | A5.3 |
| CK LOW pulse width | t_{CL} | 0.43 | 0.57 | t_{CK} | 1,3 | A5.4 |
| Address, control, and data output setup time relative to MCK rising edge | $t_{OS(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.6 |
| Address, control, and data output hold time relative to MCK rising edge | $t_{OH(base)}$ | $t_{CK}/2 - 1000$ | — | ps | 2,3 | A5.7 |
| Input data set-up time, relative to MCK | t_{IS} | 1000 | — | ps | ³ | A5.15 |
| Input data hold time, relative to MCK | t_{IH} | 1000 | — | ps | ³ | A5.16 |

NOTES:

- ¹ Measured with clock pin loaded with 50 Ω termination resistor to mid-supply.
- ² Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD_IO_MEM}/2$.
- ³ All transitions measured at mid-supply ($V_{DD_IO_MEM}/2$).

NOTE

To achieve better timing, balance the loading of DQS as MCK although DQS is not used in SDR mode.

Figure 9 shows the DDR SDRAM write timing.

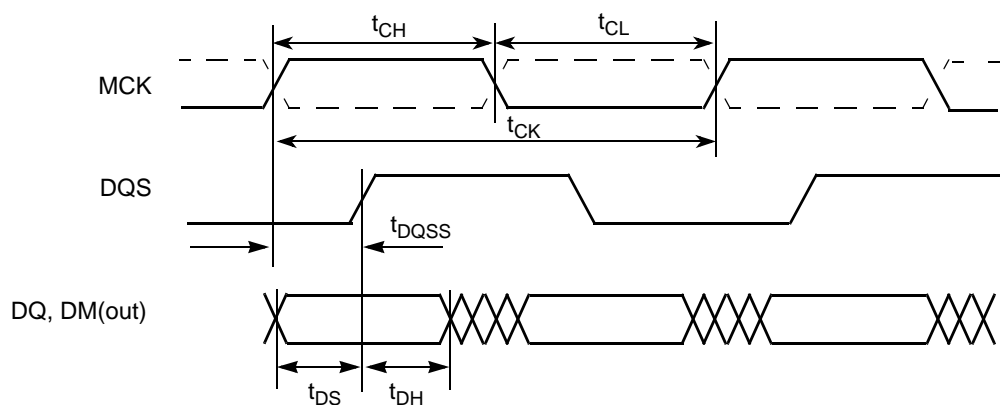


Figure 9. DDR Write Timing

Figure 10 and Figure 11 show the DDR SDRAM read timing.

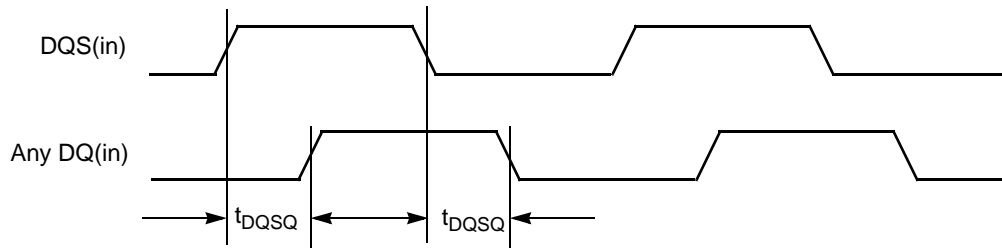


Figure 10. DDR Read Timing, DQ vs DQS

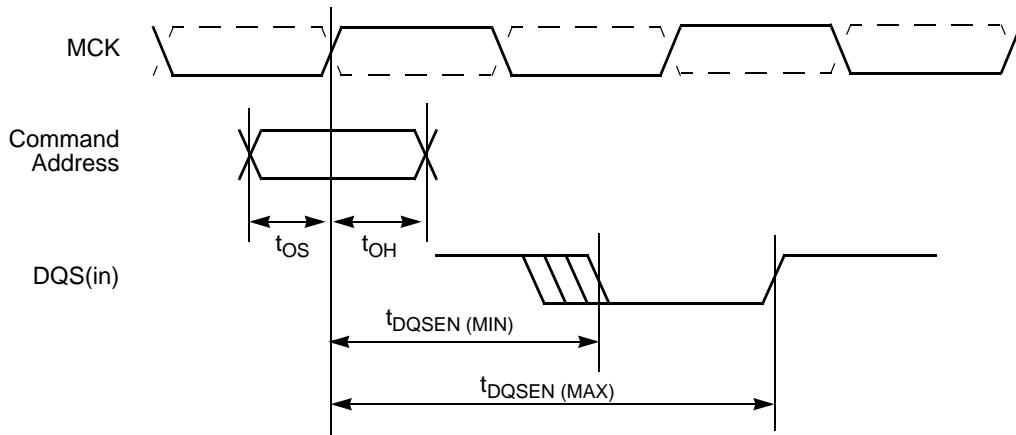


Figure 11. DDR Read Timing, DQSEN

Figure 12 shows the SDR AC timing.

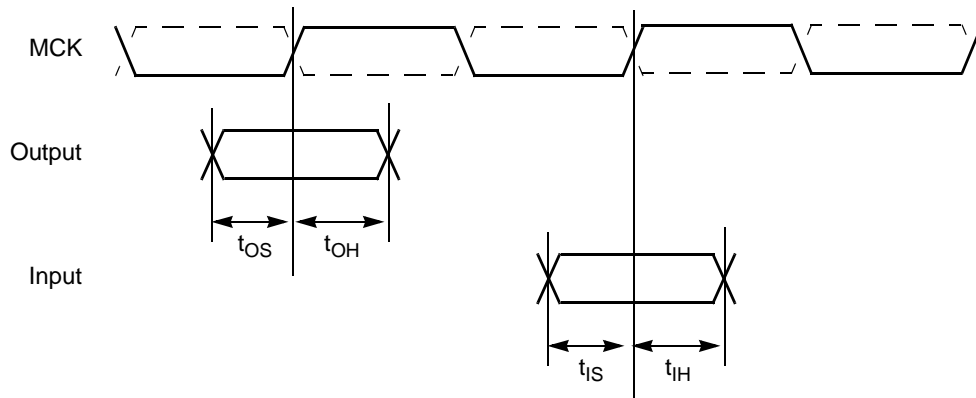


Figure 12. SDR AC Timing

Figure 13 provides the AC test load for the DDR bus.

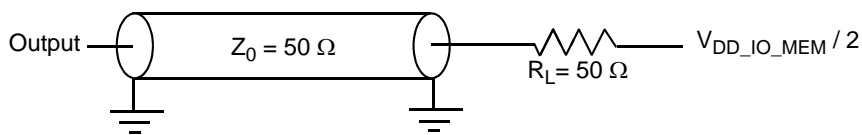


Figure 13. DDR AC Test Load

4.3.6 LPC

The local-plus bus is the external bus interface of the MPC5125. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed and MUXed. The reference clock is the LPC CLK. The maximum bus frequency is 66 MHz.

Definition of terms:

- WS = Wait state
- DC = Dead cycle
- HC = Hold cycle
- DS = Data size in bytes
- BBT =Burst bytes per transfer
- AL = Address latch enable length
- ALT = Chip select/Address Latch Timing
- t_{LPCck} = LPC clock period

Table 25. LPC Timing

| Sym | Description | Min | Max | Units | SpecID |
|----------|---|---|--|-------|--------|
| t_{OD} | $\overline{CS}[x]$, ADDR, R/\overline{W} , TSIZ, DATA (wr), \overline{TS} , \overline{OE} valid after LPC CLK (Output delay related to LPC CLK) | 0 | 5 | ns | A7.1 |
| t_1 | Non-burst $\overline{CS}[x]$ pulse width | $(2 + WS) \times t_{LPCck}$ | $(2 + WS) \times t_{LPCck}$ | ns | A7.2 |
| t_2 | ADDR, R/\overline{W} , TSIZ, DATA (wr) valid before $\overline{CS}[x]$ assertion | $t_{LPCck} - t_{OD}$ | $t_{LPCck} + t_{OD}$ | ns | A7.3 |
| t_3 | \overline{OE} assertion after $\overline{CS}[x]$ assertion | $t_{LPCck} - t_{OD}$ | $t_{LPCck} + t_{OD}$ | ns | A7.4 |
| t_4 | ADDR, R/\overline{W} , TSIZ, data (wr) hold after $\overline{CS}[x]$ negation | $t_{LPCck} - t_{OD}$ | $(HC + 1) \times t_{LPCck} + t_{OD}$ | ns | A7.5 |
| t_5 | \overline{TS} pulse width | t_{LPCck} | t_{LPCck} | ns | A7.6 |
| t_6 | DATA (rd) setup before LPC CLK | 5 | — | ns | A7.7 |
| t_7 | DATA (rd) input hold | 0 | $(DC + 1) \times t_{LPCck}$ | ns | A7.8 |
| t_8 | Read burst $\overline{CS}[x]$ pulse width | $(2 + WS + BBT/DS) \times t_{LPCck}$ | $(2 + WS + BBT/DS) \times t_{LPCck}$ | ns | A7.9 |
| t_9 | Burst \overline{ACK} pulse width | $(BBT/DS) \times t_{LPCck}$ | $(BBT/DS) \times t_{LPCck}$ | ns | A7.10 |
| t_{10} | Burst DATA (rd) input hold | 0 | — | ns | A7.11 |
| t_{11} | Read burst \overline{ACK} assertion after $\overline{CS}[x]$ assertion | $(2+WS) \times t_{LPCck}$ | $(2+WS) \times t_{LPCck}$ | ns | A7.12 |
| t_{12} | Non-MUXed write burst $\overline{CS}[x]$ pulse width | $(2.5 + WS + BBT/DS) \times t_{LPCck}$ | $(2.5 + WS + BBT/DS) \times t_{LPCck}$ | ns | A7.13 |
| t_{13} | Write burst ADDR, R/\overline{W} , TSIZ, DATA (wr) hold after $\overline{CS}[x]$ negation | $0.5 \times t_{LPCck} - t_{OD}$ | $(HC + 0.5) \times t_{LPCck} + t_{OD}$ | ns | A7.14 |
| t_{14} | Write burst \overline{ACK} assertion after $\overline{CS}[x]$ assertion | $(2.5 + WS) \times t_{LPCck} - t_{OD}$ | $(2.5 + WS) \times t_{LPCck} + t_{OD}$ | ns | A7.15 |
| t_{15} | Write burst DATA valid | $t_{LPCck} - t_{OD}$ | — | ns | A7.16 |
| t_{16} | Non-MUXed mode: asynchronous write burst ADDR valid before write DATA valid | $0.5 \times t_{LPCck} - t_{OD}$ | $0.5 \times t_{LPCck} + t_{OD}$ | ns | A7.17 |
| t_{17} | MUXed mode: ADDR cycle | $AL \times 2 \times t_{LPCck} - t_{OD}$ | $AL \times 2 \times t_{LPCck}$ | ns | A7.18 |
| t_{18} | MUXed mode: \overline{ALE} cycle | $AL \times t_{LPCck}$ | $AL \times t_{LPCck}$ | ns | A7.19 |

Table 25. LPC Timing (continued)

| Sym | Description | Min | Max | Units | SpecID |
|----------|---|--|--|-------|--------|
| t_{19} | Non-MUXed mode page burst: ADDR cycle | $t_{LPCck} - t_{OD}$ | t_{LPCck} | ns | A7.20 |
| t_{20} | Non-MUXed mode page burst: burst DATA (rd) input setup before next ADDR cycle | $t_{OD} + t_6$ | — | ns | A7.21 |
| t_{21} | Non-MUXed mode page burst: burst DATA (rd) input hold after next ADDR cycle | 0 | — | ns | A7.22 |
| t_{22} | MUXed mode: non-burst $\overline{CS}[x]$ pulse width | $(ALT \times (AL \times 2) + WS) \times t_{LPCck}$ | $(ALT \times (AL \times 2) + WS) \times t_{LPCck}$ | ns | A7.23 |
| t_{23} | MUXed mode: read-burst $\overline{CS}[x]$ pulse width | $(ALT \times (AL \times 2) + WS) + BBT/DS) \times t_{LPCck}$ | $(ALT \times (AL \times 2) + WS) + BBT/DS) \times t_{LPCck}$ | ns | A7.23 |
| t_{24} | MUXed mode: write-burst $\overline{CS}[x]$ pulse width | $(ALT \times (AL \times 2) + 2.5 WS) + BBT/DS) \times t_{LPCck}$ | $(ALT \times (AL \times 2) + 2.5 WS) + BBT/DS) \times t_{LPCck}$ | ns | A7.23 |

4.3.6.1 Non-MUXed Mode

4.3.6.1.1 Non-MUXed Non-Burst Mode

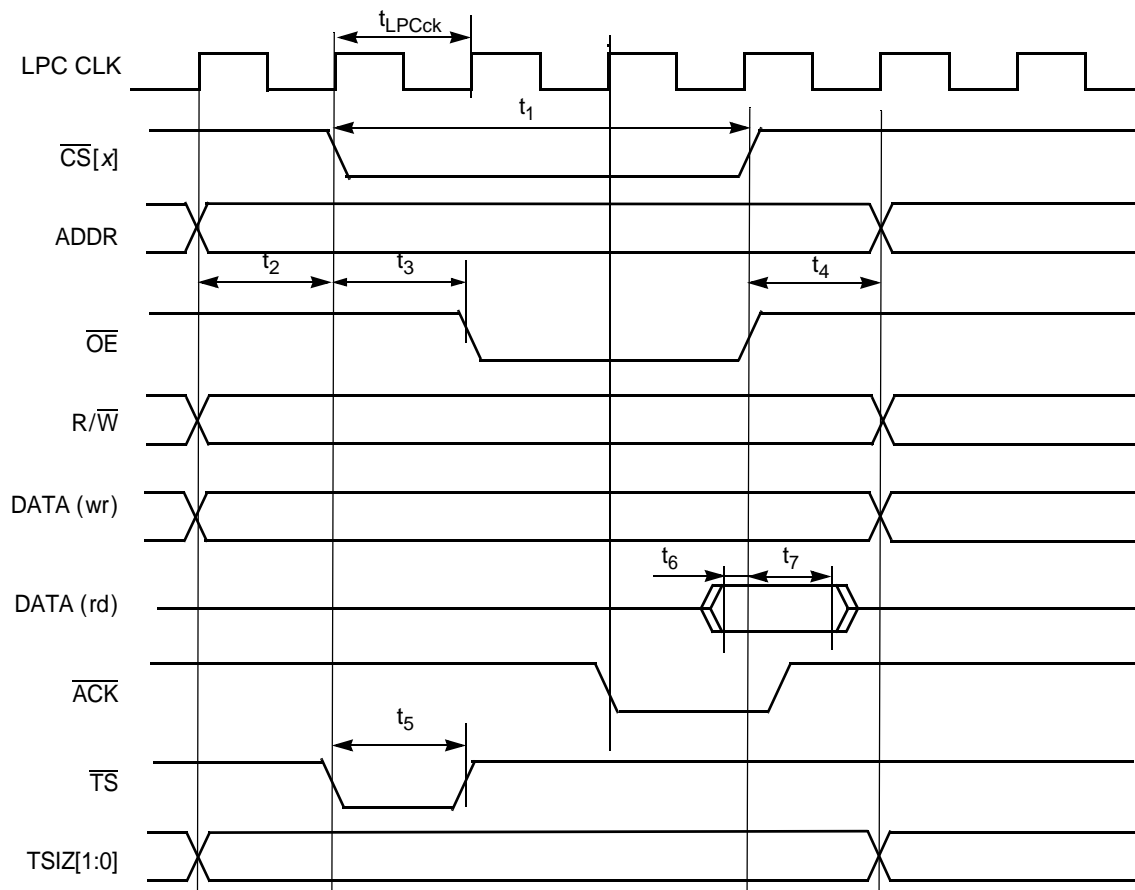


Figure 14. Timing Diagram — Non-MUXed non-Burst Mode

NOTE

$\overline{\text{ACK}}$ is asynchronous input signal and has no timing requirements. $\overline{\text{ACK}}$ needs to be deasserted after $\overline{\text{CS}}[x]$ is deasserted.

4.3.6.1.2 Non-MUXed Synchronous Read Burst Mode

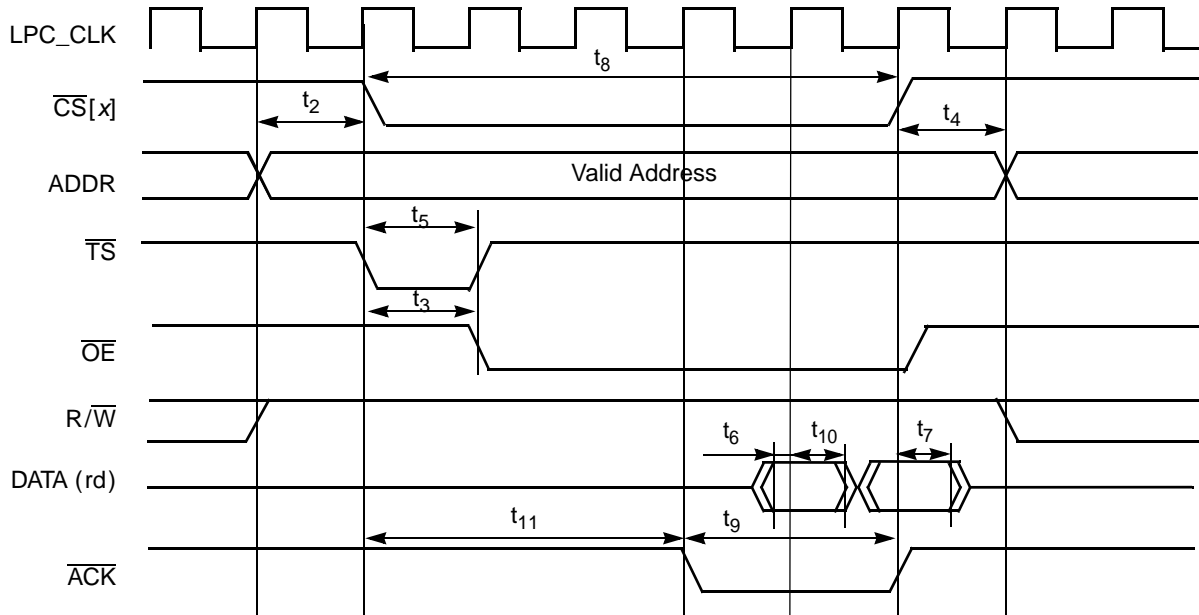


Figure 15. Timing Diagram — Non-MUXed Synchronous Read Burst Mode

4.3.6.1.3 Non-MUXed Synchronous Write Burst Mode

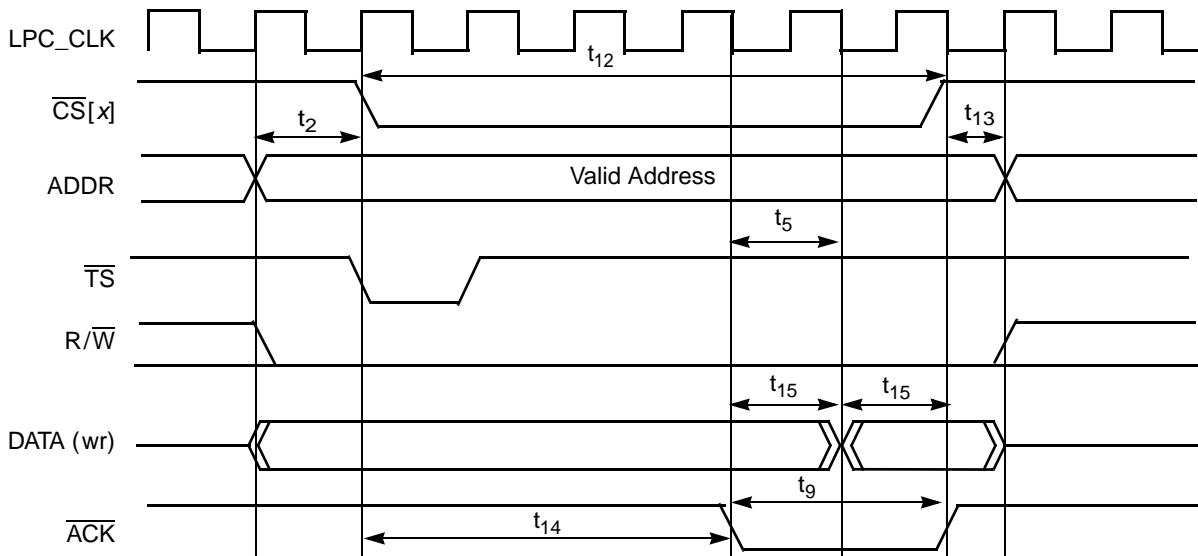


Figure 16. Timing Diagram — Non-MUXed Synchronous Write Burst

4.3.6.1.4 Non-MUXed Asynchronous Read Burst Mode (Page Mode)

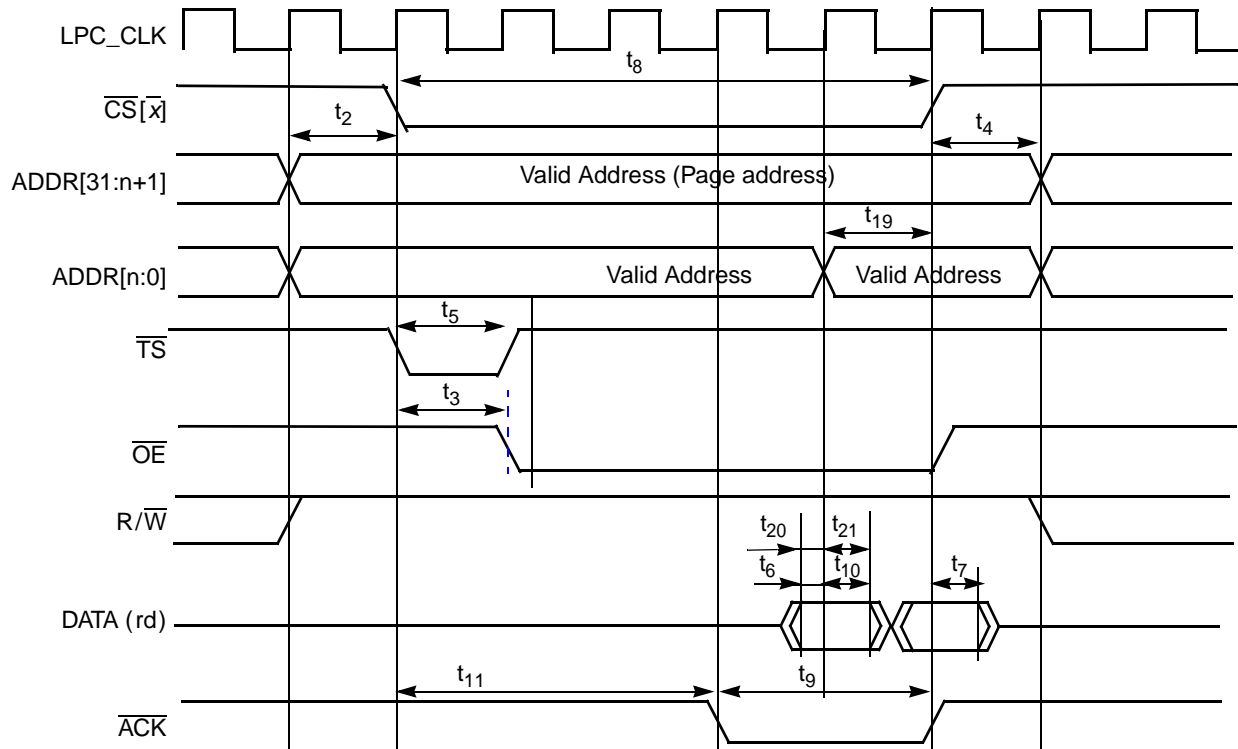


Figure 17. Timing Diagram — Non-MUXed Asynchronous Read Burst

4.3.6.1.5 Non-MUXed Asynchronous Write Burst Mode

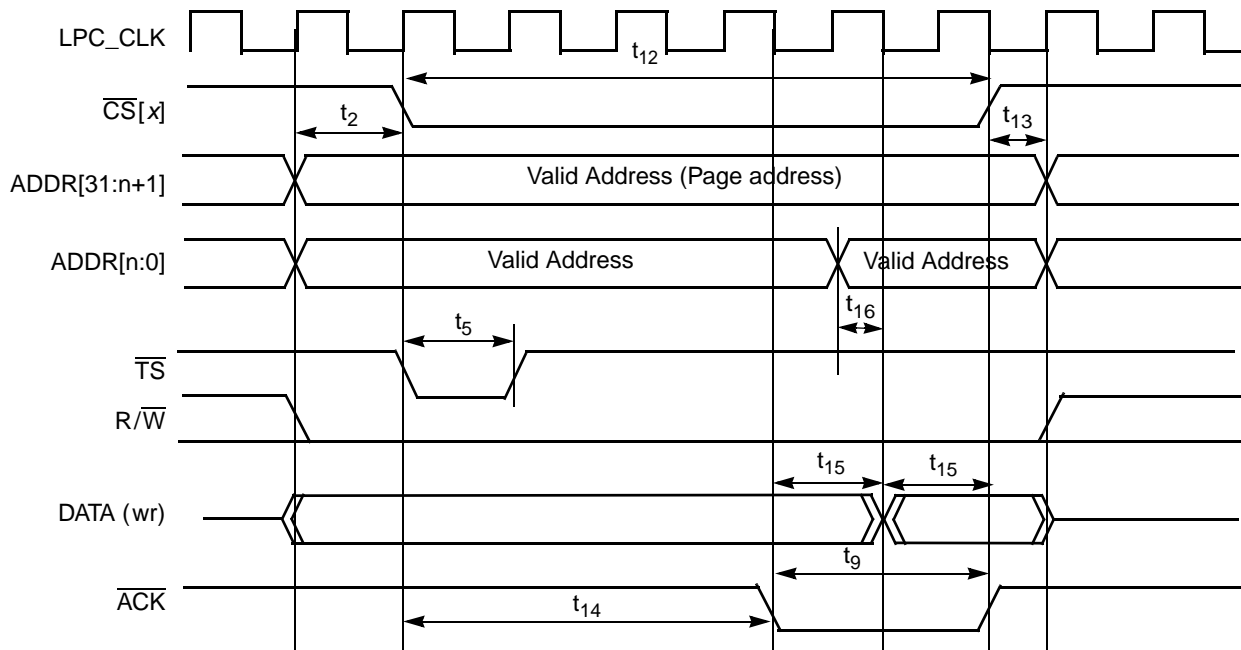


Figure 18. Timing Diagram — Non-MUXed Asynchronous Write Burst

4.3.6.2 MUXed Mode

4.3.6.2.1 MUXed Non-Burst Mode

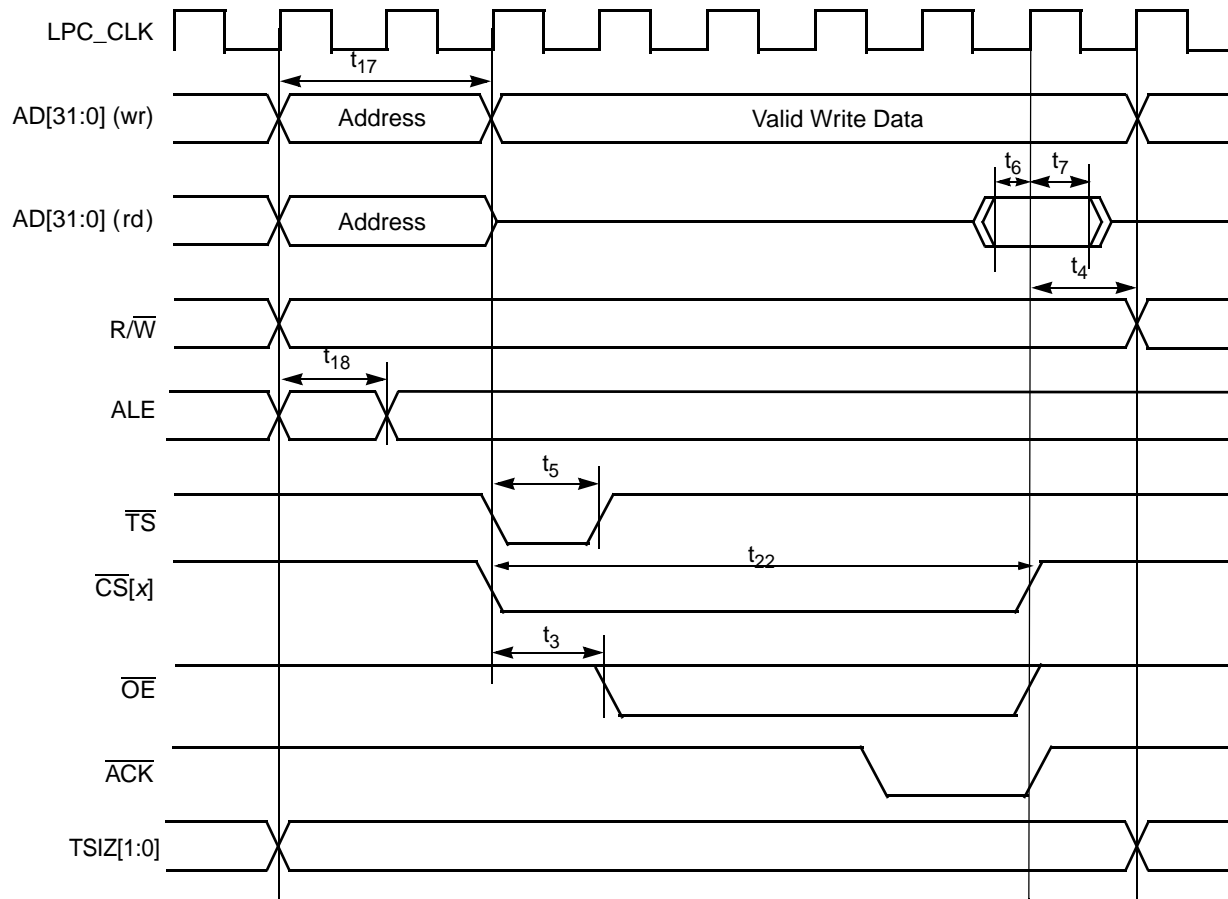


Figure 19. Timing Diagram — MUXed non-Burst Mode

NOTE

$\overline{\text{ACK}}$ is asynchronous input signal and has no timing requirements. $\overline{\text{ACK}}$ needs to be deasserted after $\overline{\text{CS}}[x]$ is deasserted.

4.3.6.2.2 MUXed Synchronous Read Burst Mode

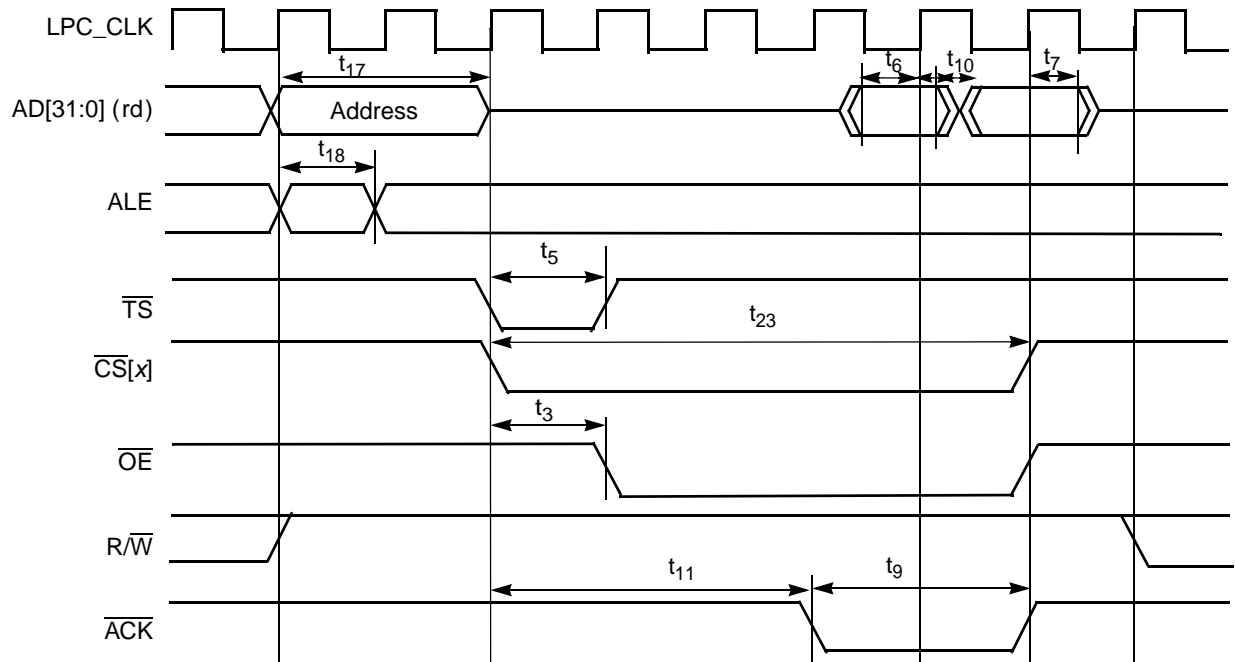


Figure 20. Timing Diagram — MUXed Synchronous Read Burst

4.3.6.2.3 MUXed Synchronous Write Burst Mode

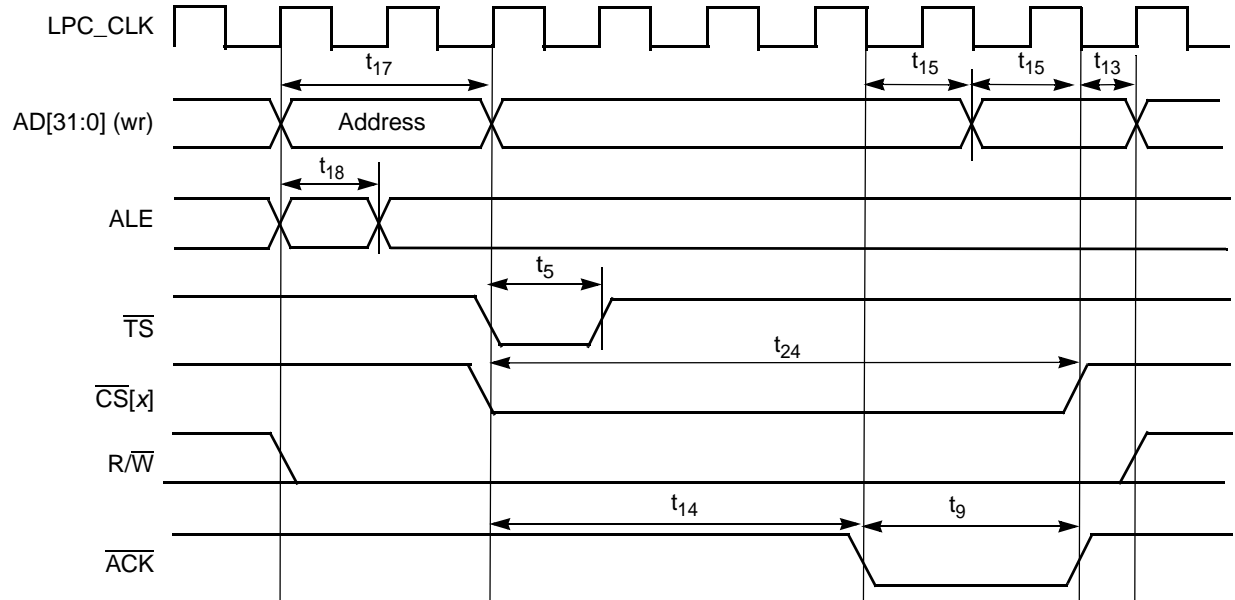


Figure 21. Timing Diagram — MUXed Synchronous Write Burst

4.3.7 NFC

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

TH is the flash clock high time, TL is flash clock low time, where

$$TH = 5 \times NFC_RATIO_H / 8 \text{ (ns)} \quad \text{Eqn. 6}$$

$$TL = 5 \times NFC_RATIO_L / 8 \text{ (ns)} \quad \text{Eqn. 7}$$

Refer to the *MPC5125 Reference Manual (MPC5125RM)* for more information about NFC_RATIO_H and NFC_RATIO_L.

Table 26. NFC Target Timing Characteristics

| Timing Parameter | Description | Min. value | Max. value | Unit | SpecID |
|------------------|---|----------------|------------|------|--------|
| t _{CLS} | NFC_CLE setup time | 2TH + TL – 1 | — | ns | A8.1 |
| t _{CLH} | NFC_CLE hold time | TH + TL – 1 | — | ns | A8.2 |
| t _{CS} | $\overline{\text{NFC_CE}}[3:0]$ setup time | 2TH + TL – 1 | — | ns | A8.3 |
| t _{CH} | $\overline{\text{NFC_CE}}[3:0]$ hold time | TH + TL | — | ns | A8.4 |
| t _{WP} | $\overline{\text{NFC_WP}}$ pulse width | TL – 1 | — | ns | A8.5 |
| t _{ALS} | NFC_ALE setup time | 2TH + TL | — | ns | A8.6 |
| t _{ALH} | NFC_ALE hold time | TH + TL | — | ns | A8.7 |
| t _{DS} | Data setup time | TL – 1 | — | ns | A8.8 |
| t _{DH} | Data hold time | TH – 1 | — | ns | A8.9 |
| t _{WC} | Write cycle time | TH + TL – 1 | — | ns | A8.10 |
| t _{WH} | $\overline{\text{NFC_WE}}$ hold time | TH – 1 | — | ns | A8.11 |
| t _{RR} | Ready to $\overline{\text{NFC_RE}}$ low | 4TH + 3TL + 90 | — | ns | A8.12 |
| t _{RP} | $\overline{\text{NFC_RE}}$ pulse width | TL + 1 | — | ns | A8.13 |
| t _{RC} | READ cycle time | TL + TH – 1 | — | ns | A8.14 |
| t _{REH} | $\overline{\text{NFC_RE}}$ high hold time | TH – 1 | — | ns | A8.15 |
| t _{IS} | Data input setup time | 6 | — | ns | A8.16 |

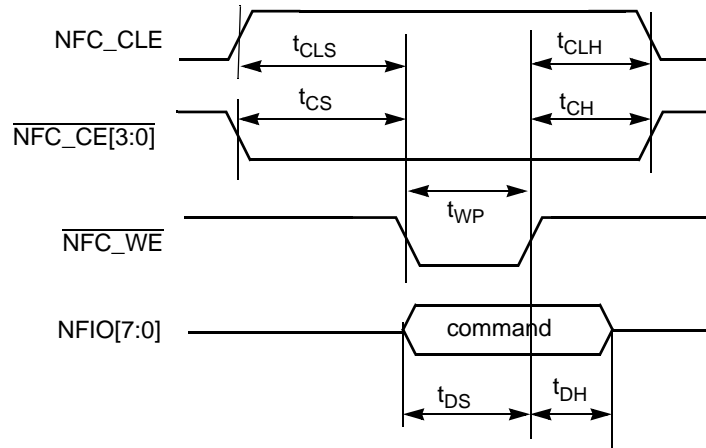


Figure 22. Command Latch Cycle Timing

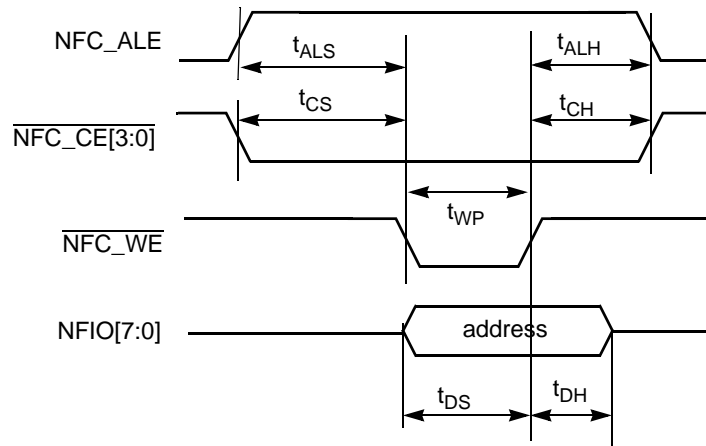


Figure 23. Address Latch Cycle Timing

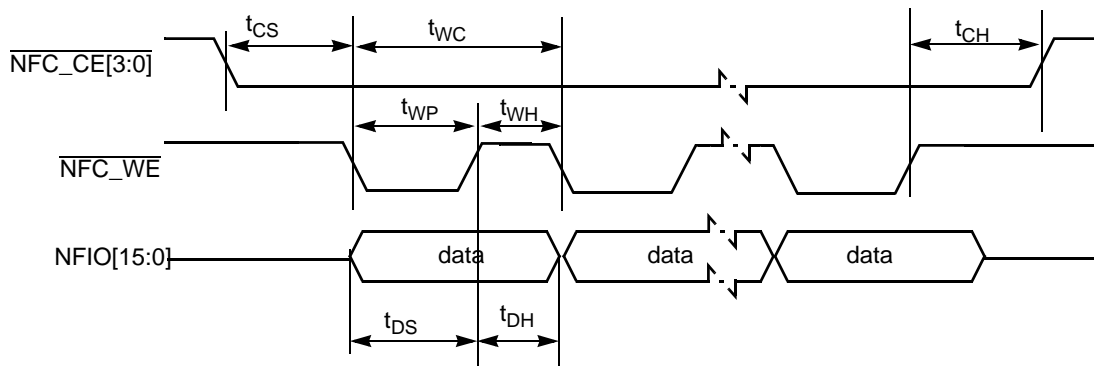


Figure 24. Write Data Latch Timing

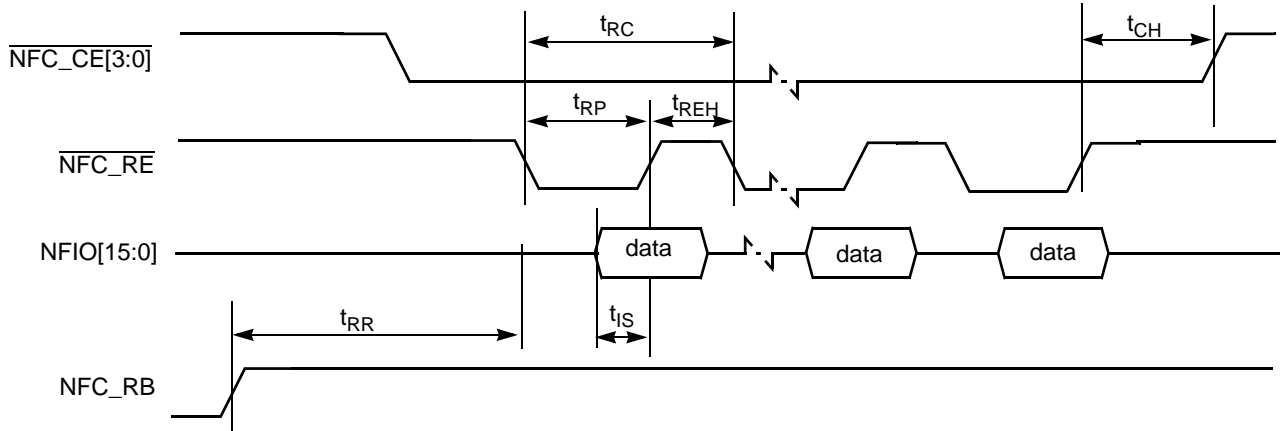


Figure 25. Read Data Latch Timing in Non-Fast Mode

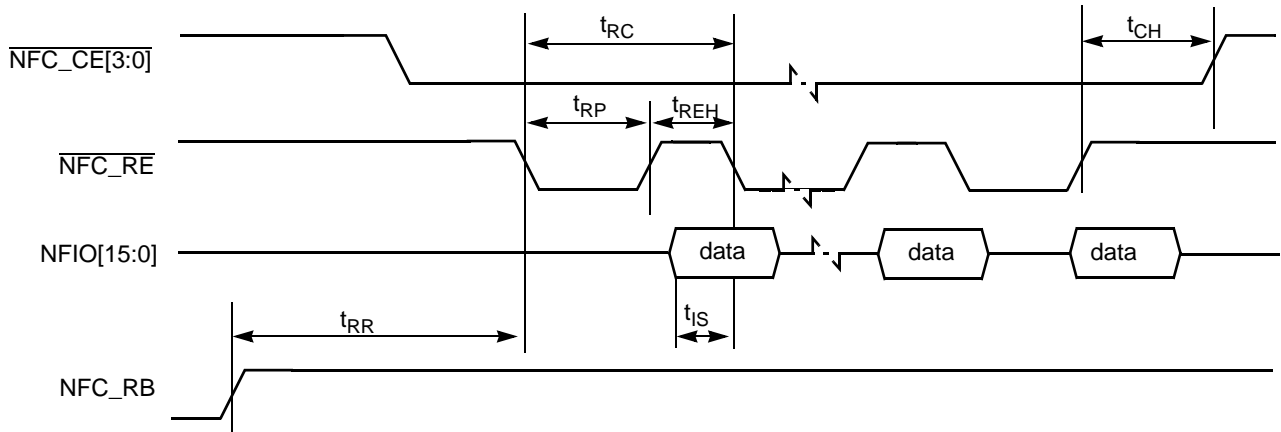


Figure 26. Read Data Latch Timing in Fast Mode

4.3.8 FEC

AC test timing conditions:

- Output Loading
All Outputs: 25 pF

Table 27. MII Rx Signal Timing

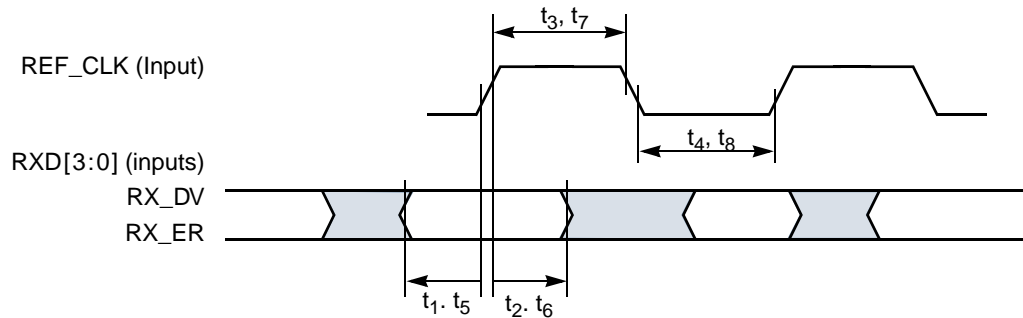
| Sym | Description | Min | Max | Unit | SpecID |
|----------------|--|-----|-----|----------------------------|--------|
| t ₁ | RXD[3:0], RX_DV, RX_ER to RX_CLK setup | 5 | — | ns | A11.1 |
| t ₂ | RX_CLK to RXD[3:0], RX_DV, RX_ER hold | 5 | — | ns | A11.2 |
| t ₃ | RX_CLK pulse width high | 35% | 65% | RX_CLK period ¹ | A11.3 |
| t ₄ | RX_CLK pulse width low | 35% | 65% | RX_CLK period ¹ | A11.4 |

NOTES:

¹ RX_CLK shall have a frequency of 25% of the data rate of the received signal. See the IEEE 802.3 specification.

Table 28. RMII Rx Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|----------------|--|-----|-----|----------------------------|--------|
| t ₅ | RXD[1:0], RX_DV, RX_ER to TX_CLK setup | 4 | — | ns | A11.5 |
| t ₆ | TX_CLK to RXD[1:0], RX_DV, RX_ER hold | 2 | — | ns | A11.6 |
| t ₇ | TX_CLK pulse width high | 35% | 65% | TX_CLK period ¹ | A11.7 |
| t ₈ | TX_CLK pulse width low | 35% | 65% | TX_CLK period ¹ | A11.8 |

NOTES:
¹ TX_CLK frequency shall be 50 MHz regardless of the data rate. See the RMII specification.


REF_CLK is TX_CLK in RMII mode, and is RX_CLK in non-RMII mode

Figure 27. Ethernet Timing Diagram — MII and RMII Rx Signal
Table 29. MII Tx Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-----------------|--|-----|-----|----------------------------|--------|
| t ₉ | TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid | 3 | — | ns | A11.9 |
| t ₁₀ | TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid | — | 25 | ns | A11.10 |
| t ₁₁ | TX_CLK pulse width high | 35% | 65% | TX_CLK Period ¹ | A11.11 |
| t ₁₂ | TX_CLK pulse width low | 35% | 65% | TX_CLK Period ¹ | A11.12 |

NOTES:
¹ The TX_CLK frequency shall be 25% of the nominal transmit frequency, for example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 specification.

Table 30. RMII Tx Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-----------------|--|-----|-----|----------------------------|--------|
| t ₁₃ | TX_CLK rising edge to TXD[1:0], TX_EN, TX_ER invalid | 3 | — | ns | A11.13 |
| t ₁₄ | TX_CLK rising edge to TXD[1:0], TX_EN, TX_ER valid | — | 14 | ns | A11.14 |
| t ₁₅ | TX_CLK pulse width high | 35% | 65% | TX_CLK Period ¹ | A11.15 |
| t ₁₆ | TX_CLK pulse width low | 35% | 65% | TX_CLK Period ¹ | A11.16 |

NOTES:
¹ TX_CLK frequency shall be 50 MHz regardless of the data rate. See the RMII specification.

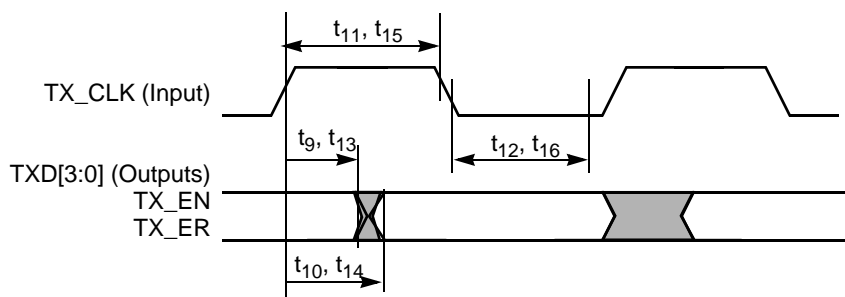


Figure 28. Ethernet Timing Diagram — MII Tx Signal

Table 31. MII Async Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-----------------|------------------------------|-----|-----|---------------|--------|
| t ₁₇ | CRS, COL minimum pulse width | 1.5 | — | TX_CLK Period | A11.17 |

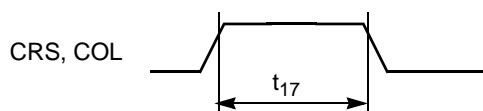


Figure 29. Ethernet Timing Diagram — MII Async

Table 32. MII Serial Management Channel Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-----------------|---------------------------------------|-----|-----|------|--------|
| t ₁₈ | MDC falling edge to MDIO output delay | 0 | 25 | ns | A11.18 |
| t ₁₉ | MDIO (input) to MDC rising edge setup | 10 | — | ns | A11.19 |
| t ₂₀ | MDIO (input) to MDC rising edge hold | 0 | — | ns | A11.20 |
| t ₂₁ | MDC pulse width high ¹ | 160 | — | ns | A11.21 |
| t ₂₂ | MDC pulse width low ¹ | 160 | — | ns | A11.22 |
| t ₂₃ | MDC period ² | 400 | — | ns | A11.23 |

NOTES:

- ¹ MDC is generated by the MPC5125 with a duty cycle of 50% except when MII_SPEED in the FEC MII_SPEED control register is changed during operation. See the *MPC5125 Reference Manual (MPC5125RM)*.
- ² The MDC period must be set to a value of less than or equal to 2.5 MHz (to be compliant with the IEEE MII characteristic) by programming the FEC MII_SPEED control register. See the *MPC5125 Reference Manual (MPC5125RM)*.

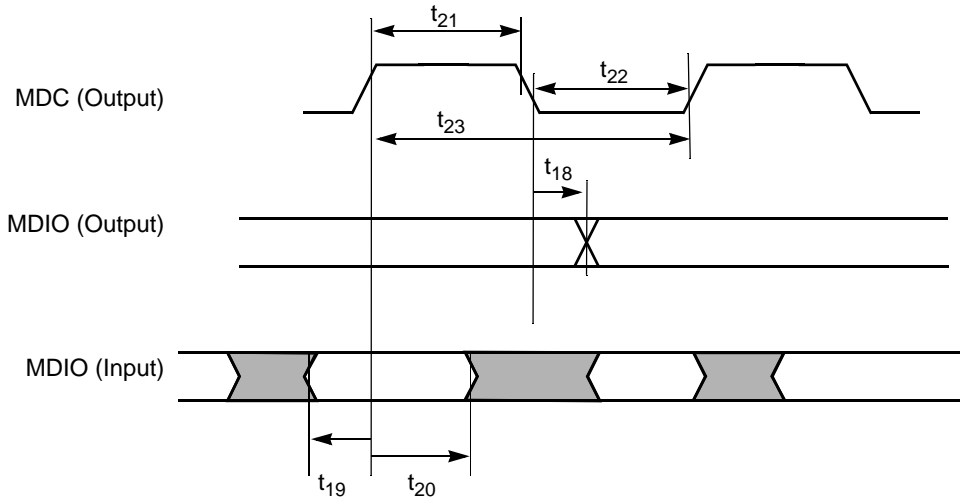


Figure 30. Ethernet Timing Diagram — MII Serial Management

4.3.9 USB ULPI

This section specifies the USB ULPI timing.

For more information refer to *UTMI+ Low Pin Interface (ULPI) Specification*, Revision 1.1, October 20, 2004.

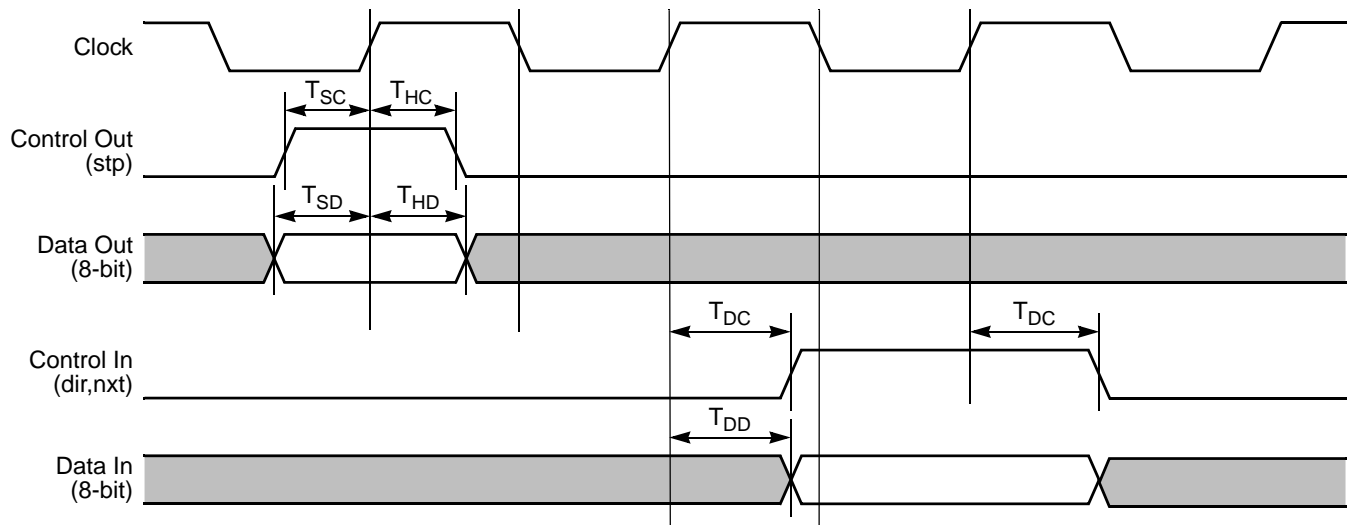


Figure 31. ULPI Timing Diagram

Table 33. Timing Specifications — USB Output Line ¹

| Sym | Description | Min | Max | Units | SpecID |
|-----------------------------------|--|-----|-----|-------|--------|
| T _{CK} | Clock period | 15 | — | ns | A12.1 |
| T _{SC} , T _{SD} | Setup time (control in, 8-bit data in) | — | 6.0 | ns | A12.2 |
| T _{HC} , T _{HD} | Hold time (control in, 8-bit data in) | 0.0 | — | ns | A12.3 |
| T _{DC} , T _{DD} | Output delay (control out, 8-bit data out) | — | 9.0 | ns | A12.4 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

4.3.10 MMC/SD/SDIO Card Host Controller (SDHC)

Figure 32 depicts the timings of the SDHC.

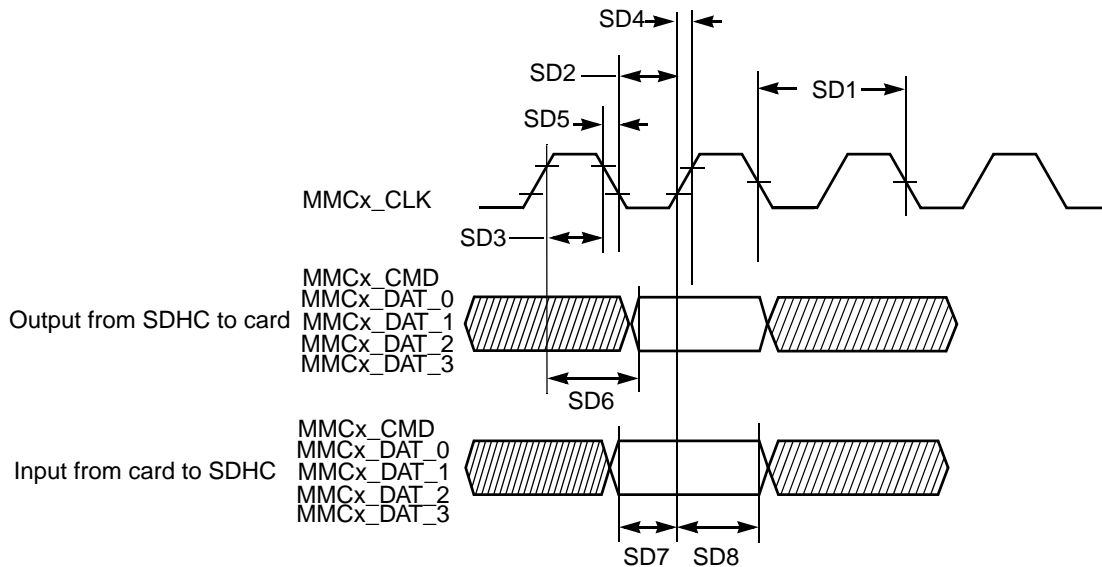


Figure 32. SDHC Timing Diagram

Table 34 lists the timing parameters.

Table 34. MMC/SD Interface Timing Parameters

| ID | Parameter | Symbols | Min | Max | Unit | SpecID |
|---|---|------------|------------|----------|------|--------|
| Card Input Clock | | | | | | |
| SD1 | Clock frequency (low speed) | f_{PP}^1 | 0 | 400 | kHz | A14.1 |
| | Clock frequency (SD/SDIO full speed/high speed) | f_{PP}^2 | 0 | 25/50 | MHz | A14.2 |
| | Clock frequency (MMC full speed/high speed) | f_{PP}^3 | 0 | 20/52 | MHz | A14.3 |
| | Clock frequency (identification mode) | f_{OD}^4 | 100 | 400 | kHz | A14.4 |
| SD2 | Clock low time (full speed/high speed) | t_{WL} | 10/7 | | ns | A14.5 |
| SD3 | Clock high time (full speed/high speed) | t_{WH} | 10/7 | | ns | A14.6 |
| SD4 | Clock rise time (full speed/high speed) | t_{TLH} | | 10/3 | ns | A14.7 |
| SD5 | Clock fall time (full speed/high speed) | t_{THL} | | 10/3 | ns | A14.8 |
| SDHC Output / Card Inputs CMD, DAT (Reference to CLK) | | | | | | |
| SD6 | SDHC output delay | t_{OD} | $TH - 3^5$ | $TH + 3$ | ns | A14.9 |
| SDHC Input / Card Outputs CMD, DAT (Reference to CLK) | | | | | | |
| SD7 | SDHC input setup time | t_{ISU} | 2.5 | | ns | A14.10 |
| SD8 | SDHC input hold time | t_{IH} | 2.5 | | ns | A14.11 |

NOTES:

- ¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
- ² In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz.
- ³ In normal data transfer mode for MMC card, clock frequency can be any value between 0–20 MHz.

- ⁴ In card identification mode, card clock must be 100 kHz ~ 400 kHz, voltage ranges from 2.7 to 3.6 V.
- ⁵ Suggested Clock Period = T, CLK_DIVIDER (in SDHC Clock Rate register) = D, then $TH = [(D + 1)/2] / (D + 1) \times T$ where [] is round.

4.3.11 DIU

The DIU is a display controller designed to manage the TFT LCD display.

4.3.11.1 Interface to TFT LCD Panels, Functional Description

Figure 33 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- DIU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DIU_CLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- DIU_HSYNC causes the panel to start a new line. It always encompasses at least one DIU_CLK pulse.
- DIU_VSYNC causes the panel to start a new frame. It always encompasses at least one DIU_HSYNC pulse.
- DIU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

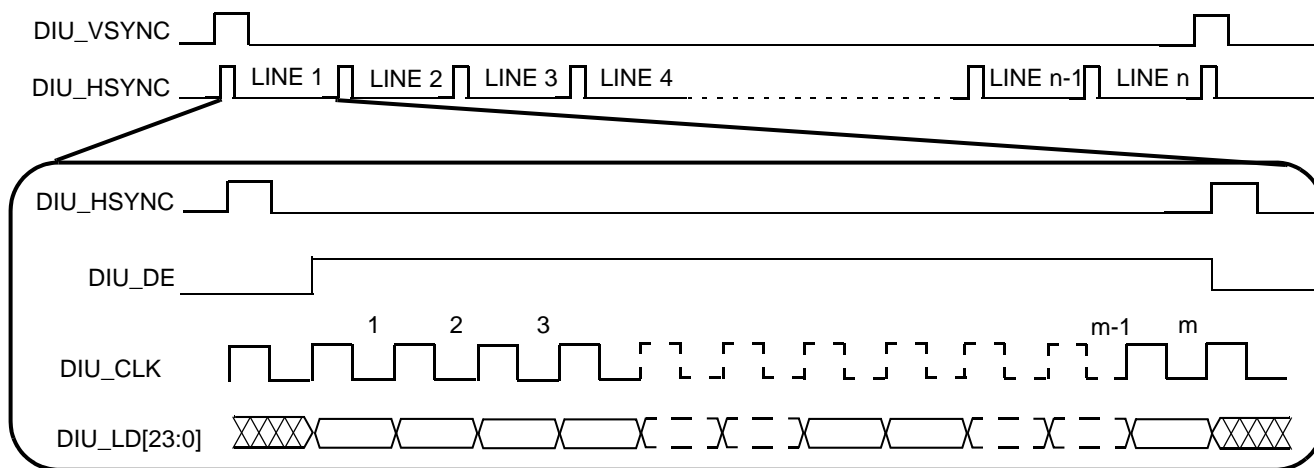


Figure 33. Interface Timing Diagram for TFT LCD Panels

4.3.11.2 Interface to TFT LCD Panels, Electrical Characteristics

Figure 34 depicts the horizontal timing (timing of one line), including the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK signal (meaning the data and sync signals change at its rising edge) and active-high polarity of the DIU_HSYNC, DIU_VSYNC, and DIU_DE signal. Signal polarity of DIU_HSYNC and DIU_VSYNC are selectable via the SYN_POL register, whether active-high or active-low. The default is active-high. The DIU_DE signal is always active-high. Also, pixel clock inversion and a flexible programmable pixel clock delay are also supported, programmed via the DIU Clock Config register (DCCR) in the system clock module.

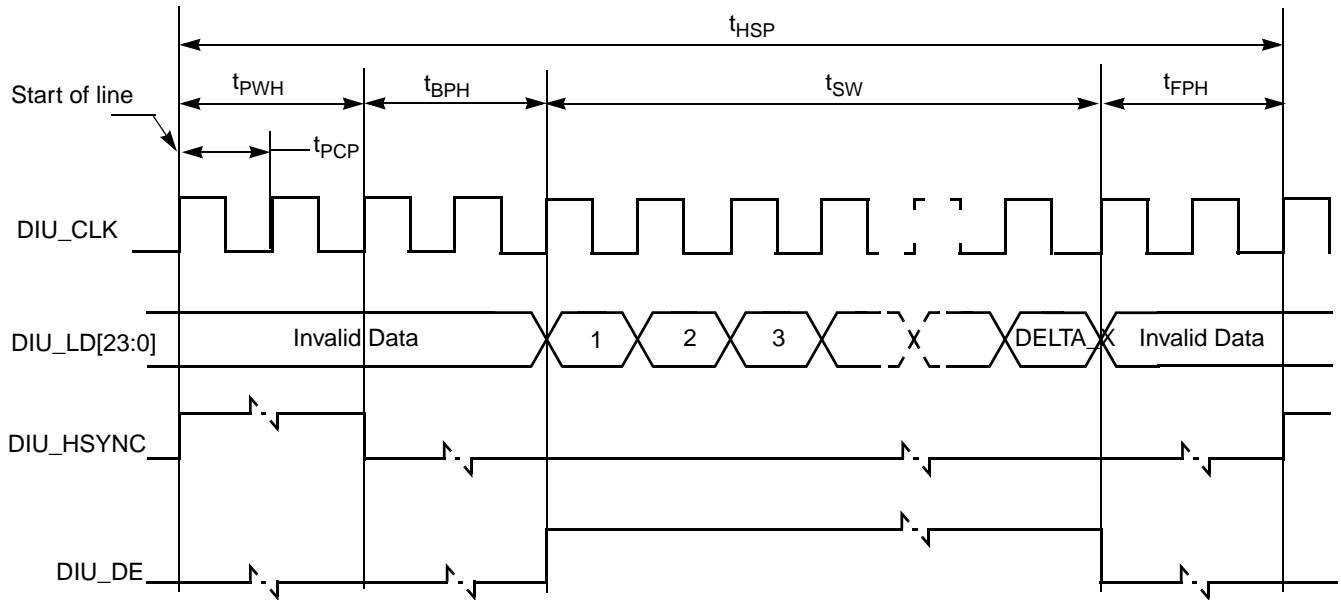


Figure 34. TFT LCD Interface Timing Diagram — Horizontal Sync Pulse

Figure 35 depicts the vertical timing (timing of one frame), including the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

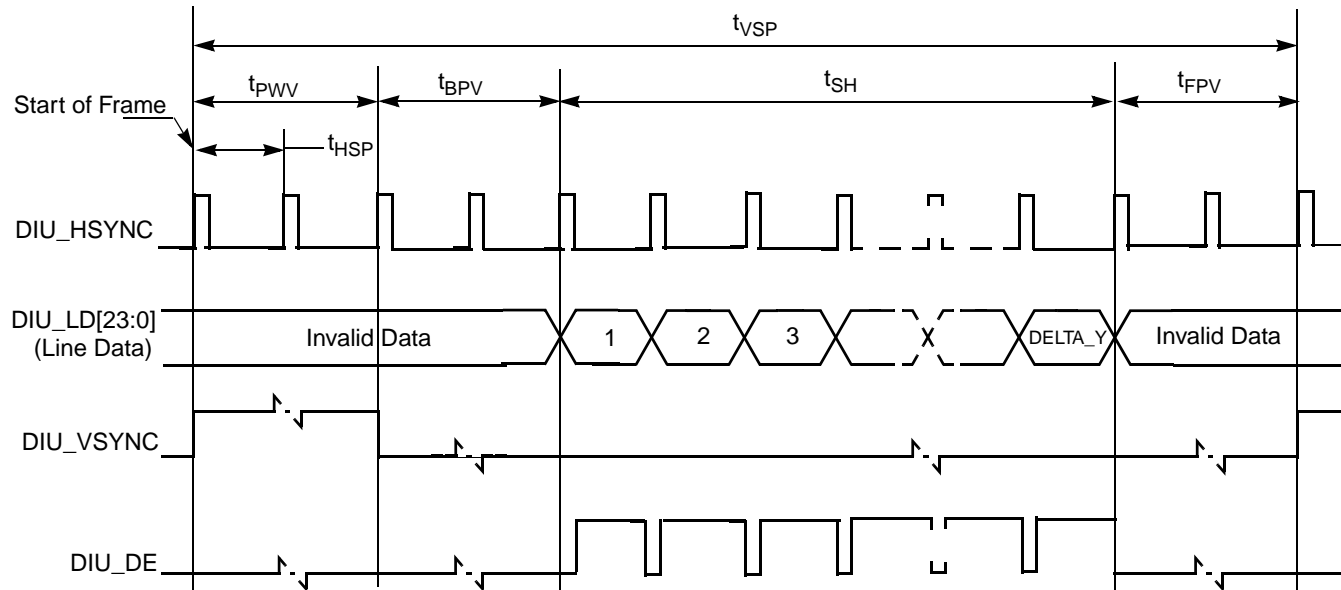


Figure 35. TFT LCD Interface Timing Diagram — Vertical Sync Pulse

Table 35 shows timing parameters of signals.

Table 35. LCD Interface Timing Parameters — Pixel Level

| Sym | Description | Value | Unit | SpecID |
|-----------|----------------------------|------------------------|------|--------|
| t_{PCP} | Display Pixel Clock Period | 15^1 | ns | A15.1 |
| t_{PWH} | HSYNC Pulse Width | $PW_H \times t_{PCP}$ | ns | A15.2 |
| t_{BPH} | HSYNC Back Porch Width | $BP_H \times t_{PCP}$ | ns | A15.3 |

Table 35. LCD Interface Timing Parameters — Pixel Level

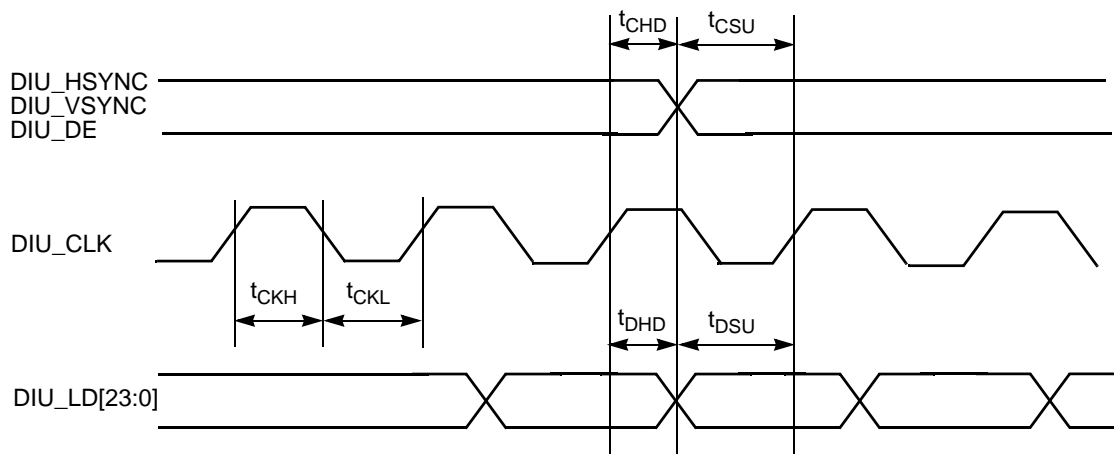
| Sym | Description | Value | Unit | SpecID |
|-----------|-------------------------|---|------|--------|
| t_{FPH} | HSYNC Front Porch Width | $FP_H \times t_{PCP}$ | ns | A15.4 |
| t_{SW} | Screen Width | $DELTA_X \times t_{PCP}$ | ns | A15.5 |
| t_{HSP} | HSYNC (Line) Period | $(PW_H + BP_H + DELTA_X + FP_H) \times t_{PCP}$ | ns | A15.6 |
| t_{PWV} | VSYNC Pulse Width | $PW_V \times t_{HSP}$ | ns | A15.7 |
| t_{BPV} | VSYNC Back Porch Width | $BP_V \times t_{HSP}$ | ns | A15.8 |
| t_{FPV} | VSYNC Front Porch Width | $FP_V \times t_{HSP}$ | ns | A15.9 |
| t_{SH} | Screen Height | $DELTA_Y \times t_{HSP}$ | ns | A15.10 |
| t_{VSP} | VSYNC (Frame) Period | $(PW_V + BP_V + DELTA_Y + FP_H) \times t_{HSP}$ | ns | A15.11 |

NOTES:

¹ Display interface pixel clock period immediate value (in nanoseconds).

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register; The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register. See appropriate section in the reference manual for detailed descriptions of these parameters.

Figure 36 depicts the synchronous display interface timing for access level, and Table 36 lists the timing parameters.


Figure 36. LCD Interface Timing Diagram — Access Level
Table 36. LCD Interface Timing Parameters — Access Level

| Parameter | Description | Min | Typ | Max | Unit | SpecID |
|-----------|---|----------------------|----------------------|----------------------|------|--------|
| t_{CKH} | LCD interface pixel clock high time | $t_{PCP} \times 0.4$ | $t_{PCP} \times 0.5$ | $t_{PCP} \times 0.6$ | ns | A15.12 |
| t_{CKL} | LCD interface pixel clock low time | $t_{PCP} \times 0.4$ | $t_{PCP} \times 0.5$ | $t_{PCP} \times 0.6$ | ns | A15.13 |
| t_{DSU} | LCD interface data setup time | 5.0 | — | — | ns | A15.14 |
| t_{DHD} | LCD interface data hold time | 6.0 | — | — | ns | A15.15 |
| t_{CSU} | LCD interface control signal setup time | 5.0 | — | — | ns | A15.16 |
| t_{CHD} | LCD interface control signal hold time | 6.0 | — | — | ns | A15.17 |

4.3.12 CAN

The CAN functions are available as TX pins at normal IO pads and as RX pins at the VBAT domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup, if configured.

4.3.13 I²C

This section specifies the timing parameters of the inter-integrated circuit (I²C) interface. Refer to the I²C bus specification.

Table 37. I²C Input Timing Specifications — SCL and SDA

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|-----|-----|---------------------------|--------|
| 1 | Start condition hold time | 2 | — | IP bus cycle ¹ | A18.1 |
| 2 | Clock low time | 8 | — | IP bus cycle ¹ | A18.2 |
| 4 | Data hold time | 0.0 | — | ns | A18.3 |
| 6 | Clock high time | 4 | — | IP bus cycle ¹ | A18.4 |
| 7 | Data setup time | 0.0 | — | ns | A18.5 |
| 8 | Start condition setup time (for repeated start condition only) | 2 | — | IP bus cycle ¹ | A18.6 |
| 9 | Stop condition setup time | 2 | — | IP bus cycle ¹ | A18.7 |

NOTES:

¹ Inter-peripheral clock is defined in the *MPC5125 Reference Manual (MPC5125RM)*

Table 38. I²C Output Timing Specifications — SCL and SDA ¹

| Sym | Description | Min | Max | Units | SpecID |
|----------------|--|-----|-----|---------------------------|--------|
| 1 ² | Start condition hold time | 6 | — | IP bus cycle ³ | A18.8 |
| 2 ² | Clock low time | 10 | — | IP bus cycle ³ | A18.9 |
| 3 ⁴ | SCL/SDA rise time | — | 7.9 | ns | A18.10 |
| 4 ² | Data hold time | 7 | — | IP bus cycle ³ | A18.11 |
| 5 ² | SCL/SDA fall time | — | 7.9 | ns | A18.12 |
| 6 ² | Clock high time | 10 | — | IP bus cycle ³ | A18.13 |
| 7 ² | Data setup time | 2 | — | IP bus cycle ³ | A18.14 |
| 8 ² | Start condition setup time (for repeated start condition only) | 20 | — | IP bus cycle ³ | A18.15 |
| 9 ² | Stop condition setup time | 10 | — | IP bus cycle ³ | A18.16 |

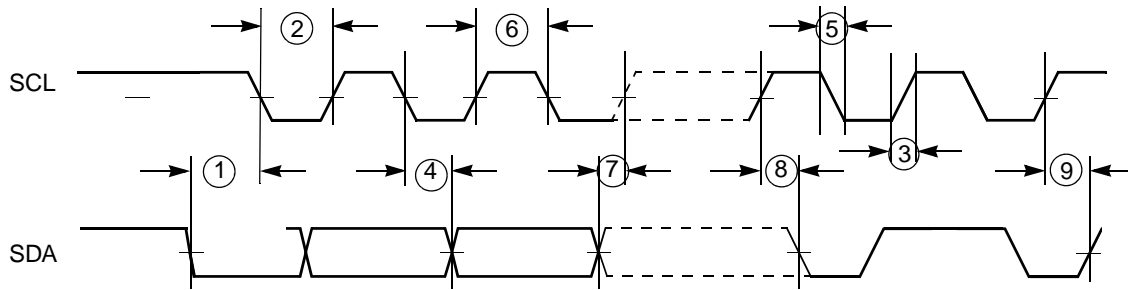
NOTES:

¹ Output timing is specified at a nominal 50 pF load.

² Programming IFDR with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

³ Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time that SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values.

⁴ Inter -peripheral Clock is defined in the *MPC5125 Reference Manual (MPC5125RM)*.


 Figure 37. Timing Diagram — I²C Input/Output

4.3.14 J1850

See the *MPC5125 Reference Manual (MPC5125RM)*.

4.3.15 PSC

The programmable serial controllers (PSC) support different modes of operation (UART, codec, AC97, SPI).

All the timing numbers specified for different PSC modes are design targets.

4.3.15.1 Codec Mode (8-, 16-, 24-, and 32-Bit) / I²S Mode

 Table 39. Timing Specifications — 8-, 16-, 24-, and 32-Bit CODEC/I²S Master Mode¹

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|--|------|-----|-----|----------------|--------|
| 1 | Bit clock cycle time, programmed in CCS register | 40.0 | — | — | ns | A20.1 |
| 2 | Clock duty cycle | 45 | 50 | 55 | % ² | A20.2 |
| 3 | Bit clock fall time | — | — | 7.9 | ns | A20.3 |
| 4 | Bit clock rise time | — | — | 7.9 | ns | A20.4 |
| 5 | FrameSync valid after clock edge | — | — | 8.4 | ns | A20.5 |
| 6 | FrameSync invalid after clock edge | — | — | 8.4 | ns | A20.6 |
| 7 | Output data valid after clock edge | — | — | 9.3 | ns | A20.7 |
| 8 | Input data setup time | 6.0 | — | — | ns | A20.8 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

² Bit clock cycle time.

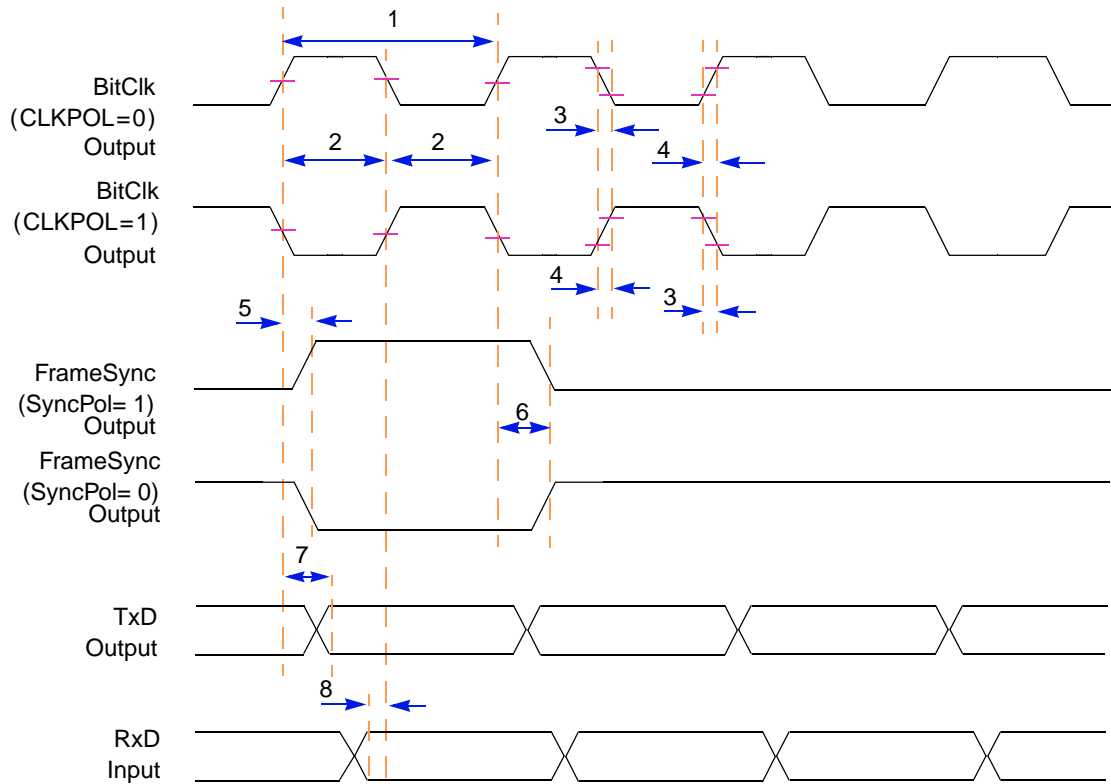


Figure 38. Timing Diagram — 8-,16-, 24-, and 32-bit CODEC/I²S Master Mode

Table 40. Timing Specifications — 8-,16-, 24-, and 32-bit CODEC/I²S Slave Mode ¹

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|------------------------------------|------|-----|------|----------------|--------|
| 1 | Bit clock cycle time | 40.0 | — | — | ns | A20.9 |
| 2 | Clock duty cycle | — | 50 | — | % ² | A20.10 |
| 3 | Frame sync setup time | 1.0 | — | — | ns | A20.11 |
| 4 | Output data valid after clock edge | — | — | 14.0 | ns | A20.12 |
| 5 | Input data setup time | 1.0 | — | — | ns | A20.13 |
| 6 | Input data hold time | 1.0 | — | — | ns | A20.14 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

² Bit clock cycle time.

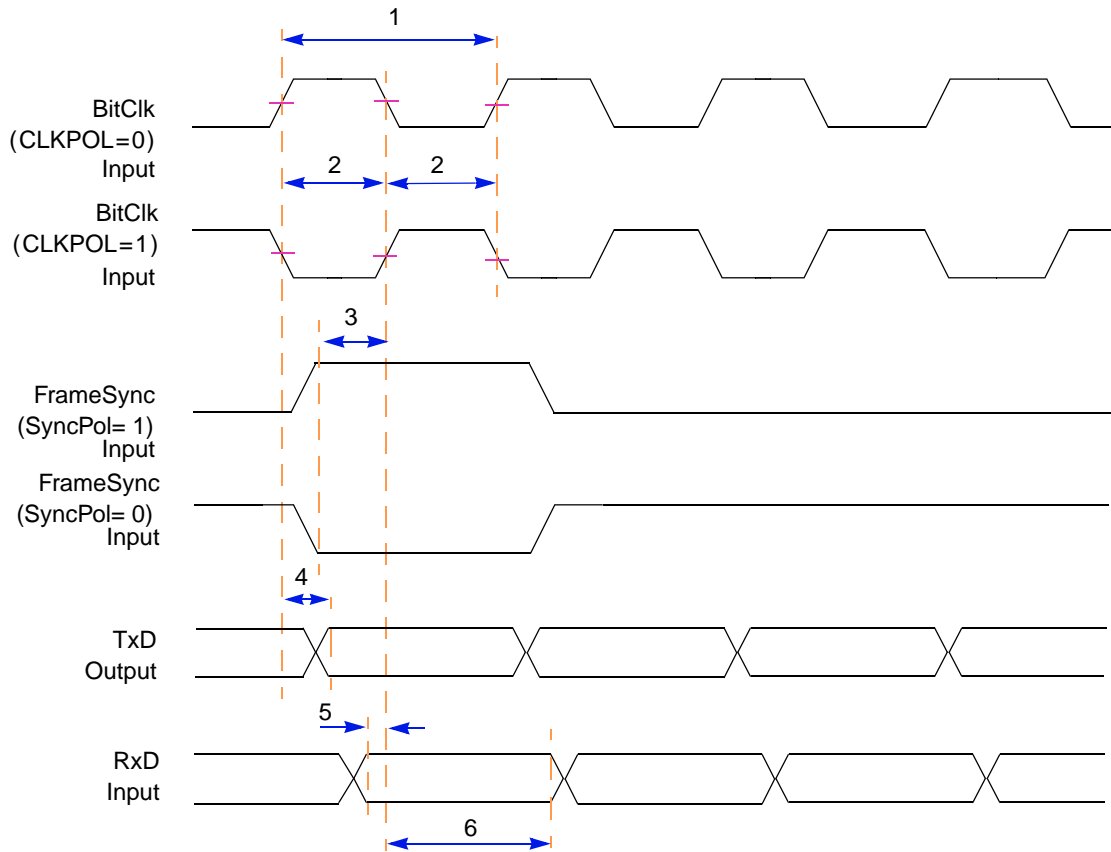


Figure 39. Timing Diagram — 8-,16-, 24-, and 32-bit CODEC/I²S Slave Mode

4.3.15.2 AC97 Mode

Table 41. Timing Specifications — AC97 Mode ¹

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|---|-----|------|------|-------|--------|
| 1 | Bit clock cycle time | — | 81.4 | — | ns | A20.15 |
| 2 | Clock pulse high time | — | 40.7 | — | ns | A20.16 |
| 3 | Clock pulse low time | — | 40.7 | — | ns | A20.17 |
| 4 | Frame sync valid after rising clock edge | — | — | 13.0 | ns | A20.18 |
| 5 | Output data valid after rising clock edge | — | — | 14.0 | ns | A20.19 |
| 6 | Input data setup time | 1.0 | — | — | ns | A20.20 |
| 7 | Input data hold time | 1.0 | — | — | ns | A20.21 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

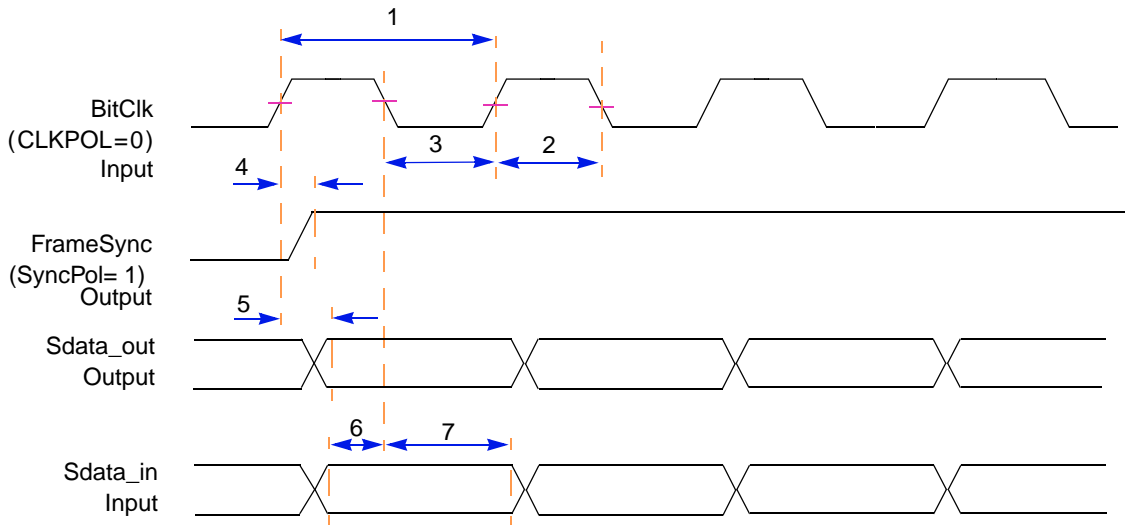


Figure 40. Timing Diagram — AC97 Mode

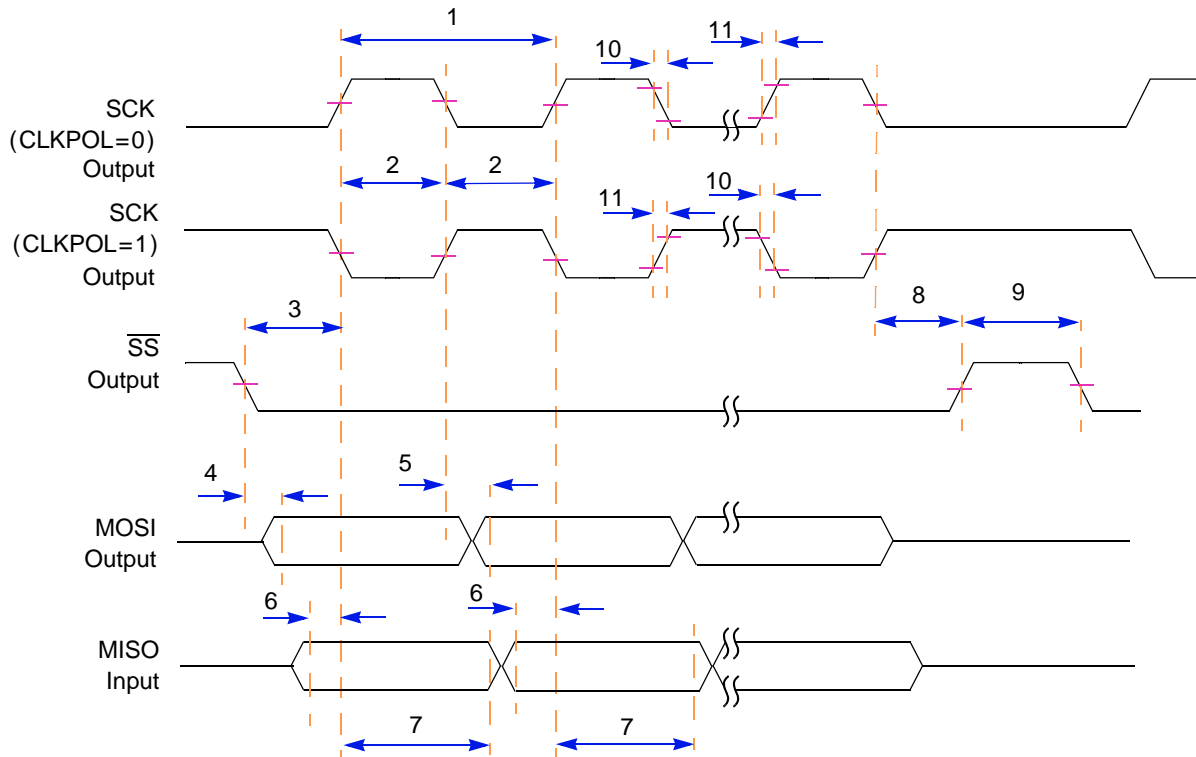
4.3.15.3 SPI Mode

Table 42. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0) ¹

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|------|------|-------|--------|
| 1 | SCK cycle time, programable in the PSC CCS register | 30.0 | — | ns | A20.26 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A20.27 |
| 3 | Slave select clock delay, programable in the PSC CCS register | 30.0 | — | ns | A20.28 |
| 4 | Output data valid after slave select (\overline{SS}) | — | 8.9 | ns | A20.29 |
| 5 | Output data valid after SCK | — | 8.9 | ns | A20.30 |
| 6 | Input data setup time | 6.0 | — | ns | A20.31 |
| 7 | Input data hold time | 1.0 | — | ns | A20.32 |
| 8 | Slave disable lag time | — | TSCK | ns | A20.33 |
| 9 | Sequential transfer delay, programable in the PSC CTUR / CTLR register | 15.0 | — | ns | A20.34 |
| 10 | Clock falling time | — | 7.9 | ns | A20.35 |
| 11 | Clock rising time | — | 7.9 | ns | A20.36 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.


Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)
Table 43. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)¹

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|------|------|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A20.37 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A20.38 |
| 3 | Slave select clock delay | 1.0 | — | ns | A20.39 |
| 4 | Input data setup time | 1.0 | — | ns | A20.40 |
| 5 | Input data hold time | 1.0 | — | ns | A20.41 |
| 6 | Output data valid after \overline{SS} | — | 14.0 | ns | A20.42 |
| 7 | Output data valid after SCK | — | 14.0 | ns | A20.43 |
| 8 | Slave disable lag time | 0.0 | — | ns | A20.44 |
| 9 | Minimum sequential transfer delay = $2 \times$ IP bus clock cycle time | 30.0 | — | — | A20.45 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

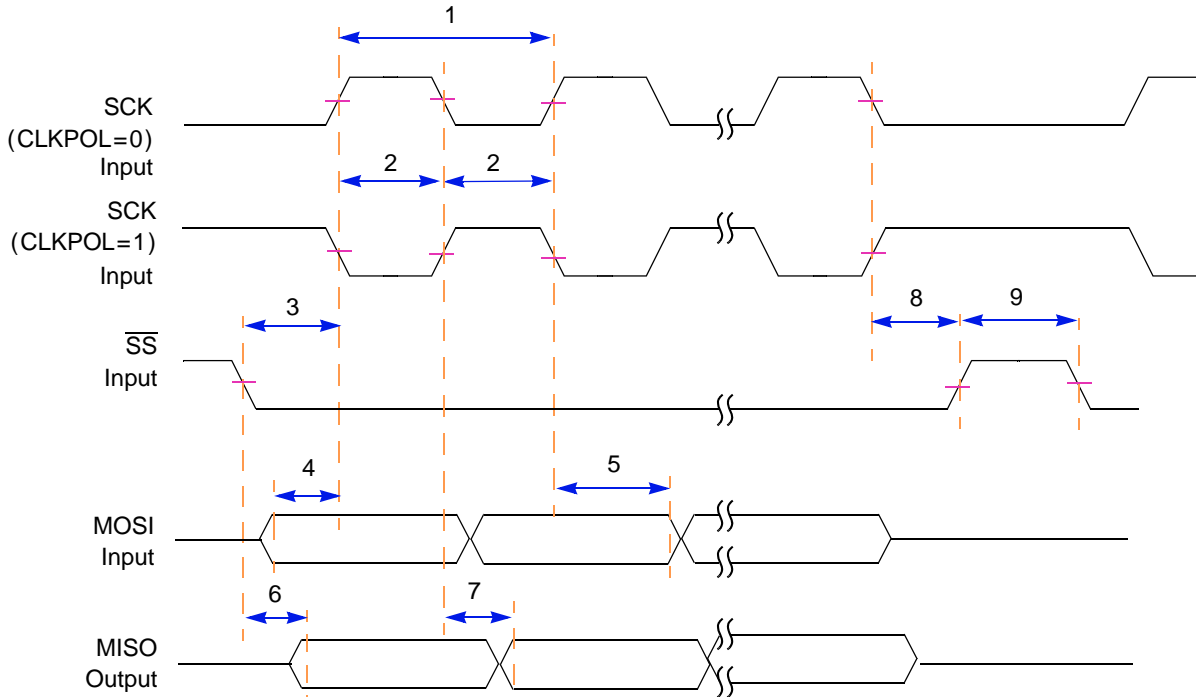


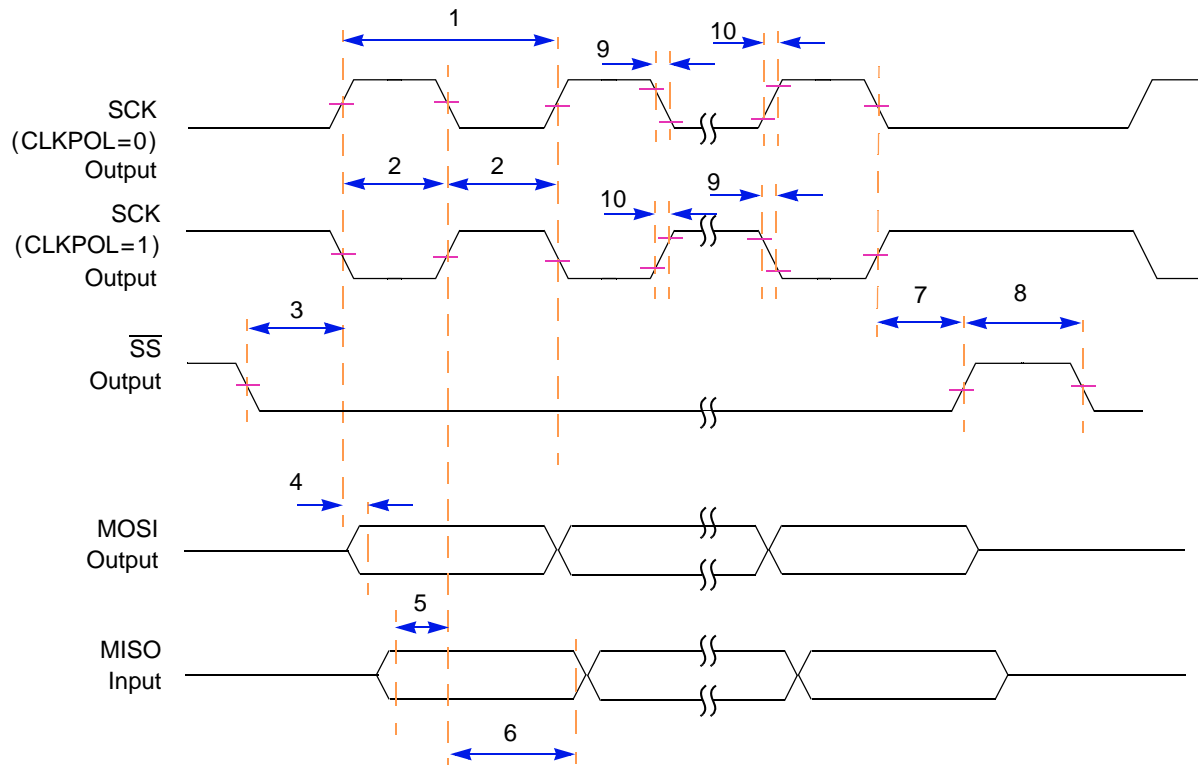
Figure 42. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 44. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1) ¹

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|------------------|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A20.46 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A20.47 |
| 3 | Slave select clock delay, programmable in the PSC CCS register | 30.0 | — | ns | A20.48 |
| 4 | Output data valid | — | 8.9 | ns | A20.49 |
| 5 | Input data setup time | 6.0 | — | ns | A20.50 |
| 6 | Input data hold time | 1.0 | — | ns | A20.51 |
| 7 | Slave disable lag time | — | T _{SCK} | ns | A20.52 |
| 8 | Sequential transfer delay, programmable in the PSC CTUR / CTLR register | 15.0 | — | ns | A20.53 |
| 9 | Clock falling time | — | 7.9 | ns | A20.54 |
| 10 | Clock rising time | — | 7.9 | ns | A20.55 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.


Figure 43. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)
Table 45. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)¹

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|------|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A20.56 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A20.57 |
| 3 | Slave select clock delay | 0.0 | — | ns | A20.58 |
| 4 | Output data valid | — | 14.0 | ns | A20.59 |
| 5 | Input data setup time | 2.0 | — | ns | A20.60 |
| 6 | Input data hold time | 1.0 | — | ns | A20.61 |
| 7 | Slave disable lag time | 0.0 | — | ns | A20.62 |
| 8 | Minimum sequential transfer delay = 2 × IP bus clock cycle time | 30.0 | — | ns | A20.63 |

NOTES:

¹ Output timing is specified at a nominal 50 pF load.

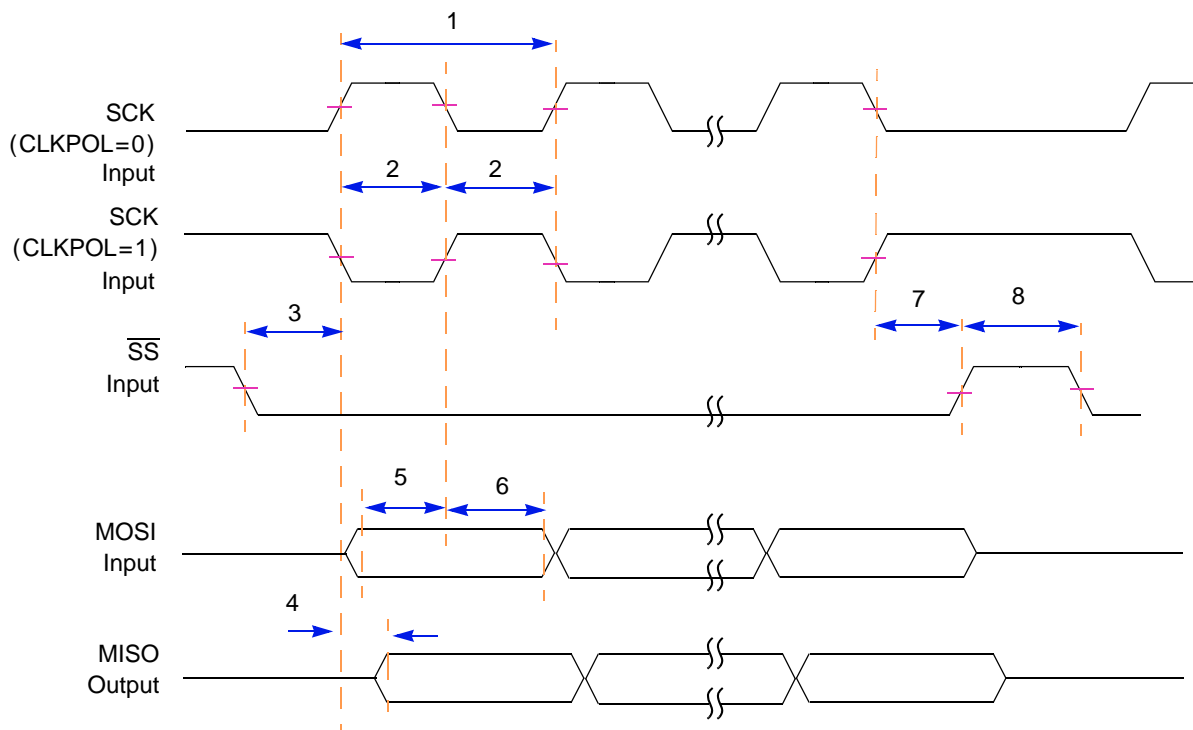


Figure 44. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

4.3.16 GPIOs and Timers

The MPC5125 contains several sets of I/Os that do not require special setup, hold, or valid requirements. The external events (GPIO or timer inputs) are asynchronous to the system clock. The inputs must be valid for at least t_{IOWID} to ensure proper capture by the internal IP clock.

Table 46. GPIO/Timers Input AC Timing Specifications

| Symbol | Description | Min | Unit | SpecID |
|-------------|--|--------|------|--------|
| t_{IOWID} | GPIO/Timers inputs — minimum pulse width | $2T^1$ | ns | A21.1 |

NOTES:

¹ T is the IP bus clock cycle. T = 15 ns is the minimum value (for the maximum IP bus frequency of 66 MHz).

4.3.17 Fusebox

Table 47 gives the Fusebox timing specification.

Table 47. Fusebox Timing Characteristics

| Sym | Description | Min | Max | Units | SpecID |
|--------------|---|------|-----|---------|--------|
| t_{FUSEWR} | Program time ¹ for fuse | 62.5 | — | μ s | A22.1 |
| I_{FUSEWR} | Program current to program one fuse bit | — | 10 | mA | A22.2 |

NOTES:

¹ The program length is defined by the value defined in the EPM_PGM_LENGTH bits of the IIM module.

4.3.18 IEEE 1149.1 (JTAG)

Table 48. JTAG Timing Specification

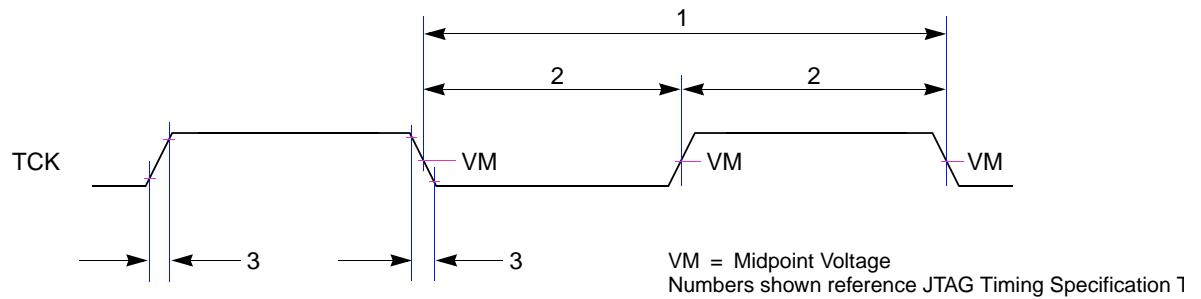
| Sym | Characteristic | Min | Max | Unit | SpecID |
|-----|--|------|-----|------|--------|
| — | TCK frequency of operation | 0 | 25 | MHz | A23.1 |
| 1 | TCK cycle time | 40 | — | ns | A23.2 |
| 2 | TCK clock pulse width measured at 1.5 V | 1.08 | — | ns | A23.3 |
| 3 | TCK rise and fall times | 0 | 3 | ns | A23.4 |
| 4 | $\overline{\text{TRST}}$ setup time to TCK falling edge ¹ | 10 | — | ns | A23.5 |
| 5 | $\overline{\text{TRST}}$ assert time | 5 | — | ns | A23.6 |
| 6 | Input data setup time ² | 5 | — | ns | A23.7 |
| 7 | Input data hold time ² | 15 | — | ns | A23.8 |
| 8 | TCK to output data valid ³ | 0 | 30 | ns | A23.9 |
| 9 | TCK to output high impedance ³ | 0 | 30 | ns | A23.10 |
| 10 | TMS, TDI data setup time | 5 | — | ns | A23.11 |
| 11 | TMS, TDI data hold time | 4.5 | — | ns | A23.12 |
| 12 | TCK to TDO data valid | 0 | 15 | ns | A23.13 |
| 13 | TCK to TDO high impedance | 0 | 15 | ns | A23.14 |

NOTES:

¹ $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

² Non-test, other than TDI and TMS, signal input timing with respect to TCK.

³ Non-test, other than TDO, signal output timing with respect to TCK.


Figure 45. Timing Diagram — JTAG Clock Input

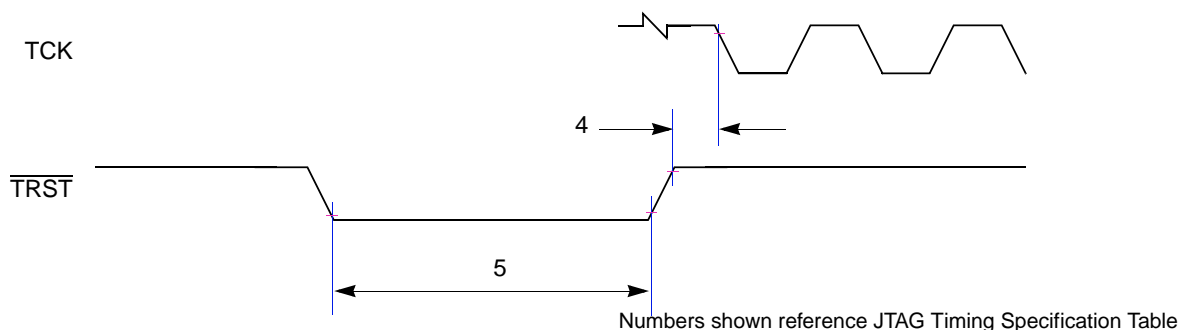


Figure 46. Timing Diagram — JTAG TRST

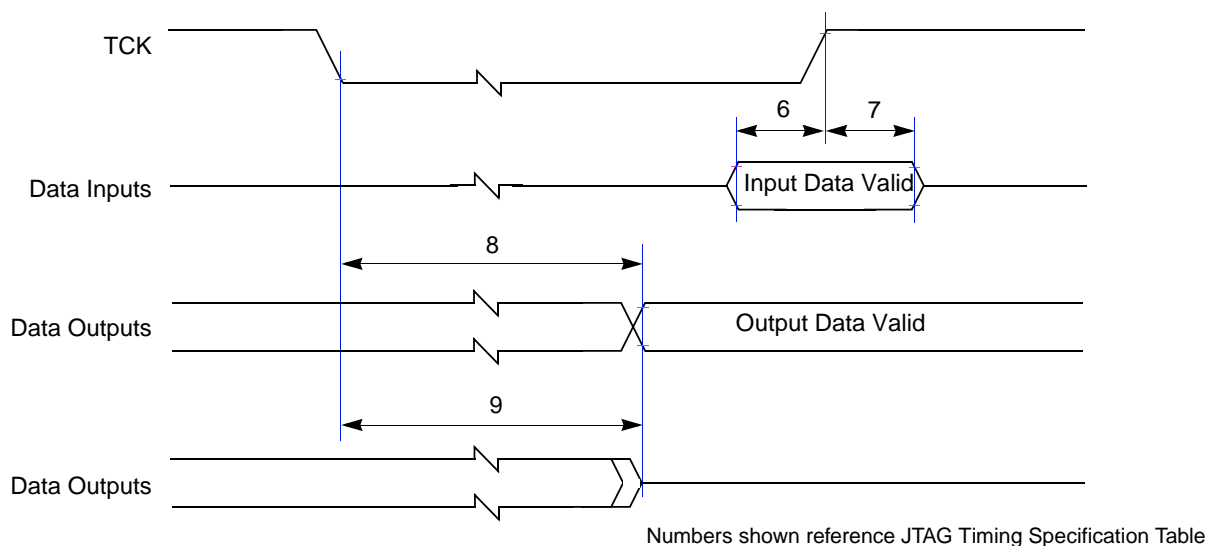


Figure 47. Timing Diagram — JTAG Boundary Scan

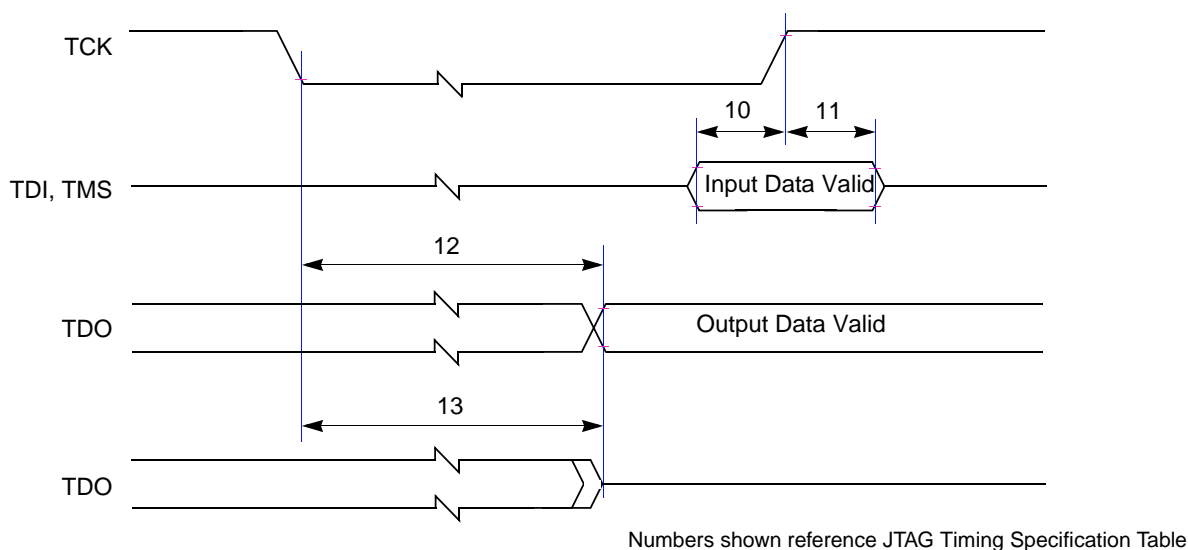


Figure 48. Timing Diagram — Test Access Port

5 System Design Information

5.1 Power Up/Down Sequencing

Power sequencing between the 1.4 V power supply V_{DD} and the remaining supplies is required to prevent excessive current during power-up phase.

The required power sequence is as follows:

- Use 12 V/ms or slower time for all supplies.
- Power up V_{DD_IO} , AV_{DD_PLLS} , V_{BAT} (if not applied permanently), and $V_{DD_IO_MEM}$ supplies first in any order, and then power up V_{DD} . If required AV_{DD_FUSEWR} should be powered up afterwards.
- All the supplies must reach the specified operating conditions before the $\overline{PORESET}$ can be released.
- For power down, drop AV_{DD_FUSEWR} to 0 V first, drop V_{DD} to 0 V, and then drop all other supplies.
- V_{DD} should not exceed V_{DD_IO} , $V_{DD_IO_MEM}$, V_{BAT} , or AV_{DD_PLLS} by more than 0.4 V at any time, including power-up.

5.2 System and CPU Core AV_{DD} Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. Figure 49 shows a recommendation for the required filter circuit.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

All traces should be as low impedance as possible, especially ground pins to the ground plane.

The filter for system/core PLLVDD to V_{SS} should be connected to the power and ground planes, respectively, not fingers of the planes.

In addition to keeping the filter components for system/core PLLVDD as close as practical to the body of the MPC5125 as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the MPC5125.

The capacitors for C2 in the figure below should be rated X5R or better due to temperature performance. It is recommended to add a bypass capacitance of at least 1 μF for the VBAT pin.

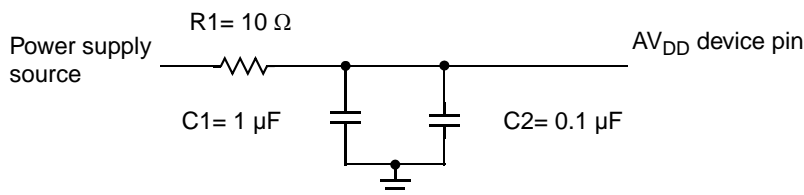


Figure 49. Power Supply Filtering

5.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD_IO} . Unused active high inputs should be connected to V_{SS} . All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} and V_{SS} pins of the MPC5125.

The unused AV_{DD_FUSEWR} power should be connected to V_{SS} directly or via a resistor.

For DDR or LPDDR modes, the unused pins VTT[3:0] for DDR2 termination voltage can be unconnected.

5.4 Pullup/Pulldown Resistor Requirements

The MPC5125 requires external pullup or pulldown resistors on certain pins.

5.4.1 Pulldown Resistor Requirements for TEST Pin

The MPC5125 requires a pulldown resistor on the test pin TEST.

5.5 JTAG

The MPC5125 has an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a common on-chip processor (COP) interface, which shares the IEEE 1149.1 JTAG port.

The COP interface provides access to the MPC5125's embedded e300 processor and to other on-chip resources. This interface provides a means for executing test routines and for performing software development and debug functions.

5.5.1 JTAG_TRST

Boundary scan testing is enabled through the JTAG interface signals. The JTAG_TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the Power Architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

5.5.1.1 TRST and PORESET

The JTAG interface can control the direction of the MPC5125 I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5125 comes out of power-on reset; do this by asserting TRST before PORESET is released.

For more details, see the Reset and JTAG Timing Specification.



Figure 50. $\overline{\text{PORESET}}$ vs. $\overline{\text{TRST}}$

5.5.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

5.5.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5125 functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale standard COP/BDM interface. Table 49 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 49. COP/BDM Interface Signals

| BDM Pin # | I/O Pin | BDM Connector | Internal Pullup/Pulldown | External Pullup/Pulldown | I/O ¹ |
|-----------|--------------------------------|---------------------|--------------------------|--------------------------|------------------|
| 16 | — | GND | — | — | — |
| 15 | $\overline{\text{CKSTP_OUT}}$ | ckstp_out | — | 10 k Ω Pullup | I |
| 14 | — | KEY | — | — | — |
| 13 | $\overline{\text{HRESET}}$ | hreset | Pullup | 10 k Ω Pullup | O |
| 12 | — | GND | — | — | — |
| 11 | $\overline{\text{SRESET}}$ | sreset | Pullup | 10 k Ω Pullup | O |
| 10 | — | N/C | — | — | — |
| 9 | TMS | tms | Pullup | 10 k Ω Pullup | O |
| 8 | $\overline{\text{CKSTP_IN}}$ | ckstp_in | — | 10 k Ω Pullup | O |
| 7 | TCK | tck | Pullup | 10 k Ω Pullup | O |
| 6 | — | VDD ² | — | — | — |
| 5 | See Note ³ | halted ³ | — | — | I |
| 4 | $\overline{\text{TRST}}$ | trst | Pullup | 10 k Ω Pullup | O |
| 3 | TDI | tdi | Pullup | 10 k Ω Pullup | O |
| 2 | See Note ^{pci_frame} | qack ⁴ | — | — | O |
| 1 | TDO | tdo | — | — | I |

NOTES:

¹ With respect to the emulator tool's perspective:
 Input is really an output from the embedded e300 core.
 Output is really an input to the core.

² From the board under test, power sense for chip power.

³ HALTED is not available from e300 core.

For a board with a COP (common on-chip processor) connector that accesses the JTAG interface and needs to reset the JTAG module, it is not recommended to wire only $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$.

To reset the MPC5125 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5125. The circuitry shown in Figure 51 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ separately, while any other board sources can drive $\overline{\text{PORESET}}$.

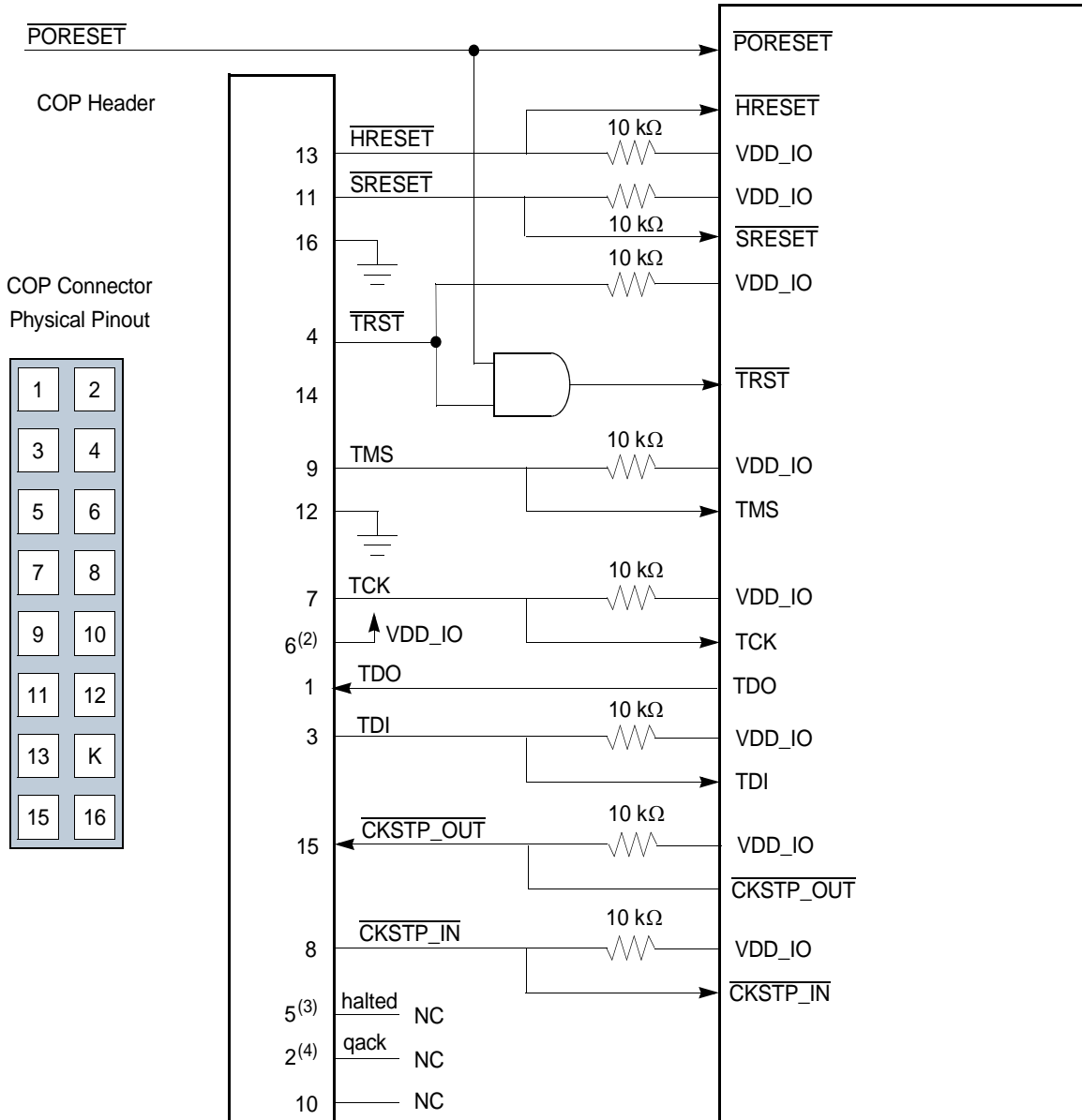


Figure 51. COP Connector Diagram

5.5.2.2 Boards Without COP Connector

If the JTAG interface is not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$, so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 52 shows the connection of the JTAG interface without COP connector.

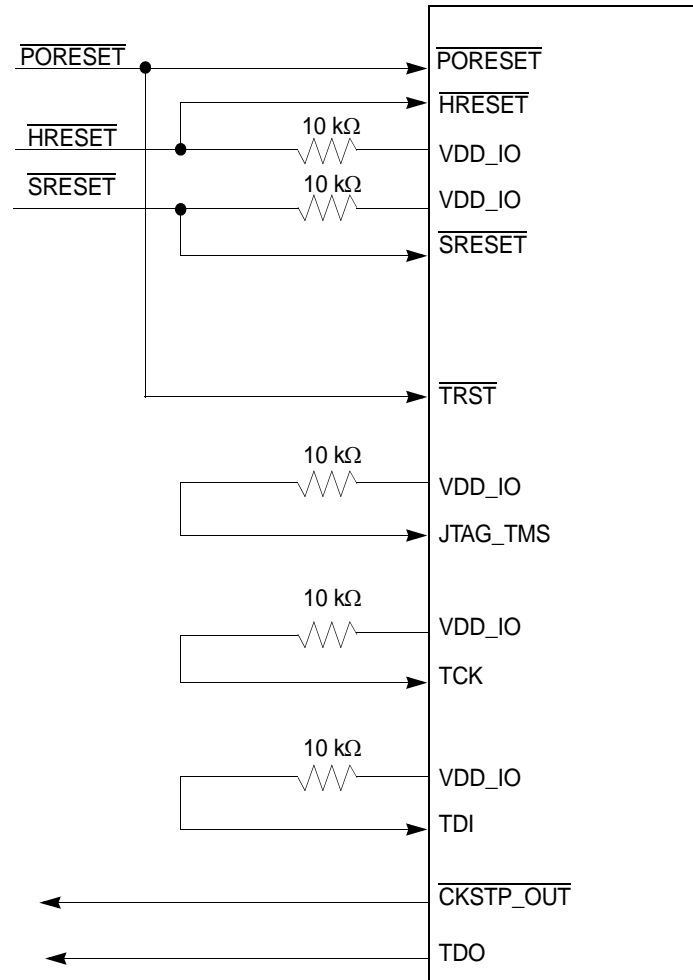


Figure 52. $\overline{\text{TRST}}$ Wiring for Boards without COP Connector

6 Package Information

This section details package parameters and dimensions. The MPC5125 is available in a thermally enhanced plastic ball grid array (TEPBGA). [Section 6.1, “Package Parameters,”](#) and [Section 6.2, “Mechanical Dimensions,”](#) provide information on the TEPBGA.

6.1 Package Parameters

Table 50. TEPBGA Parameters

| | |
|-------------------------|------------------------------------|
| Package outline | 23 mm × 23 mm |
| Interconnects | 324 |
| Pitch | 1.00 mm |
| Module height (typical) | 2.25 mm |
| Solder balls | 96.5 Sn/3.5Ag (VN <i>package</i>) |
| Ball diameter (typical) | 0.6 mm |

6.2 Mechanical Dimensions

Figure 3 shows the mechanical dimensions and bottom surface nomenclature of the MPC5125 324 TEPBGA package.

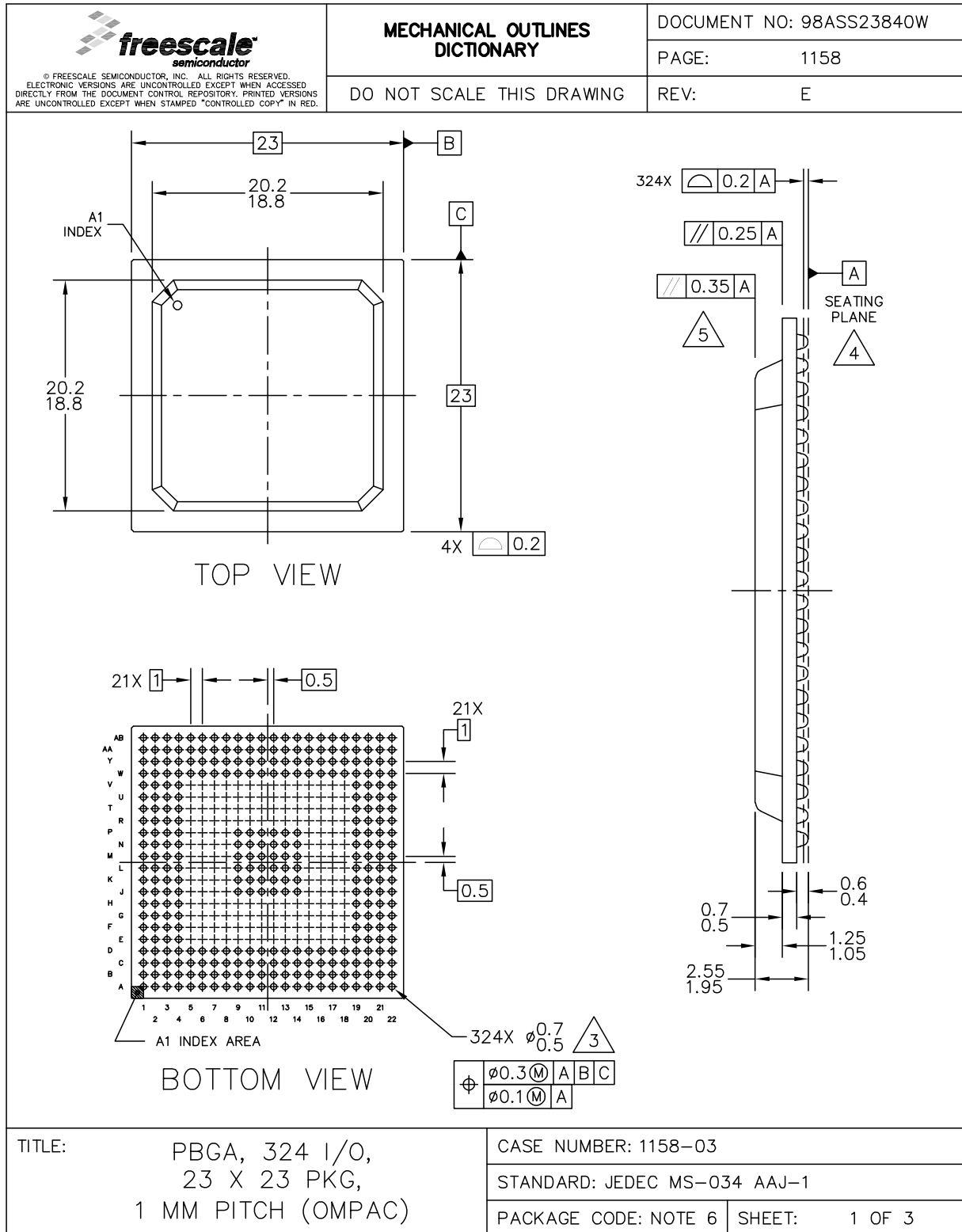


Figure 53. Mechanical Drawing of MPC5125 PBGA (1 of 3)

Package Information

| | | | |
|---|--|------------------------------|----------|
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| <p>NOTES:</p> <ol style="list-style-type: none"> 1. ALL DIMENSIONS IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A. 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS. 5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE. 6. PACKAGE CODES: 5241: 2 LAYER 324 PBGA 5366: 4 LAYER 324 TEPBGA PGE | | | |
| TITLE: | PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC) | CASE NUMBER: 1158-03 | |
| | | STANDARD: JEDEC MS-034 AAJ-1 | |
| | | PACKAGE CODE: NOTE 6 | SHEET: 2 |

Figure 54. Mechanical Drawing of MPC5125 PBGA (2 of 3)

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| | | | STANDARD: JEDEC MS-034 AAJ-1 | | |
| | | | PACKAGE CODE: NOTE 6 | SHEET: | 3 |

Figure 55. Mechanical Drawing of MPC5125 PBGA (3 of 3)

7 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: <http://www.freescale.com> .

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5125 Microprocessor Reference Manual* (document number MPC5125RM)
- *MPC5125 (0M01S) Errata* (document number MSE5125_0M01S)

8 Revision History

Table 51 describes the changes made to this document between revisions.

Table 51. Revision History

| Revision | Date | Description |
|----------|---------------|--|
| 1 | October 2008 | Initial public release, NDA required, Advance Information. |
| 2 | October 2009 | Public release, Technical Data. <ul style="list-style-type: none"> — Updated specifications according to characterized data. — Updated Table 1, orderable part numbers. — Updated Table 2, pin multiplexing. — Editorial updates. |
| 3 | November 2009 | Public release, Technical Data. <ul style="list-style-type: none"> — Corrected part number. |
| 4 | August 2011 | Public release, Technical Data. <ul style="list-style-type: none"> — Incorporated TKT052929. Updated Table 2, "pin multiplexing". FEC1_TX_CLK I/O direction changed from O to I. — Incorporated TKT052932. Updated Table 2, "pin multiplexing". NFC_R/B changed to NFC_R/B0 for ALT0 of NFC_RB ; the ALT2 function of the PSC1_3 signal lists NFC_R/B2 signal direction changed as an input; the ALT2 function of the J1850_RX signal lists NFC_R/B3 signal direction changed as an input. — Incorporated TKT068361. Updated Table 2, "pin multiplexing". FEC1_TX_ER I/O direction changed from I to O, FEC1_MDC I/O direction changed from I to O, FEC2_TX_ER changed from I to O, FEC2_MDC I/O direction changed from I to O. — Updated Table 2, "pin multiplexing". "ALT3" replaced with "ALT2" for "RST_CONF" (reset configuration); FEC1_MDIO/RMII_MDIO I/O direction changed from I to I/O ; FEC_TX_EN I/O direction changed to O from I; USB1_DATA1 and USB1_NEXT I/O direction changed to O from I — Updated Table 6, "DC Electrical Specifications". The unit of "RODT" changed to 'ohm' from 'W'. |

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